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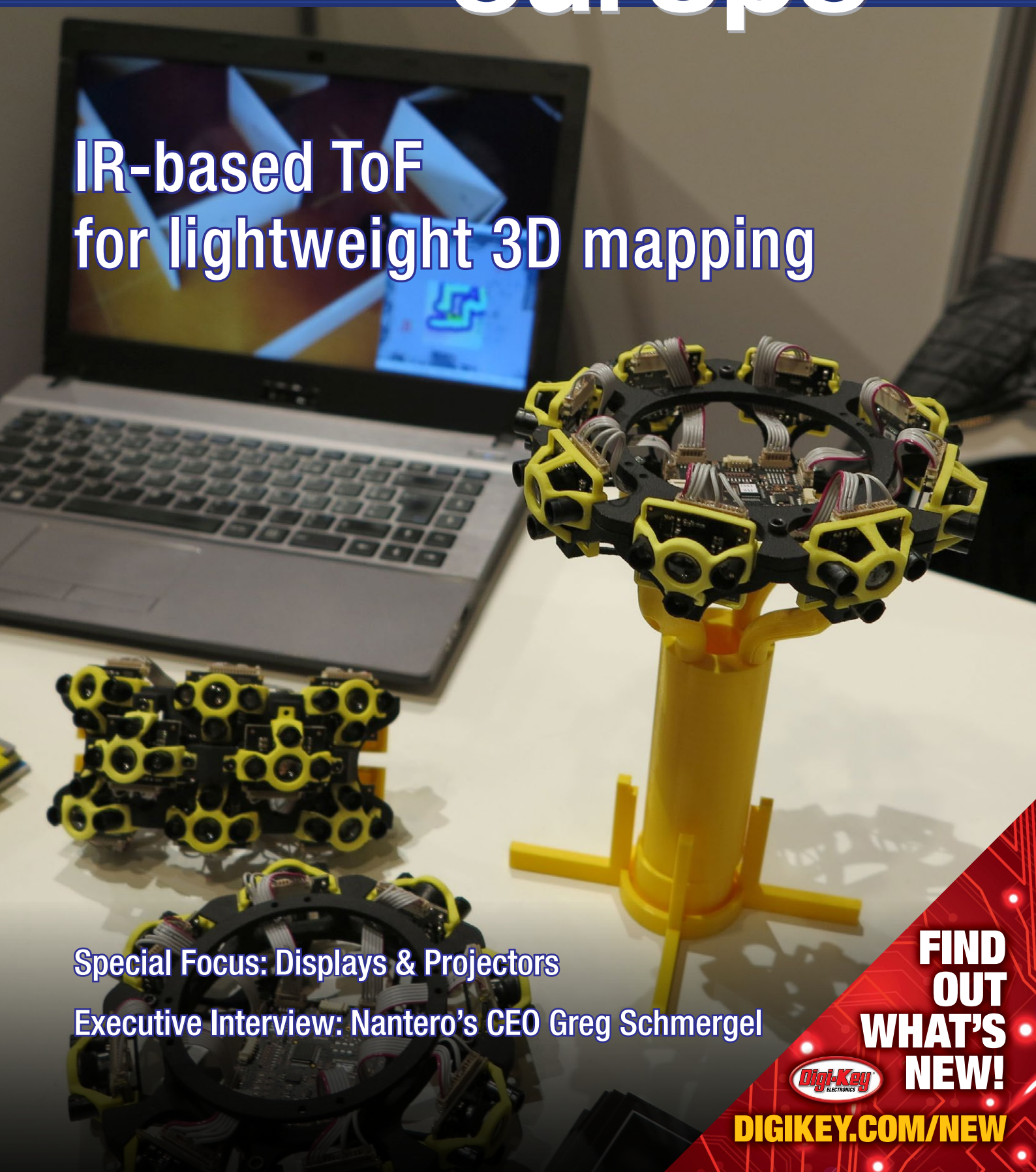

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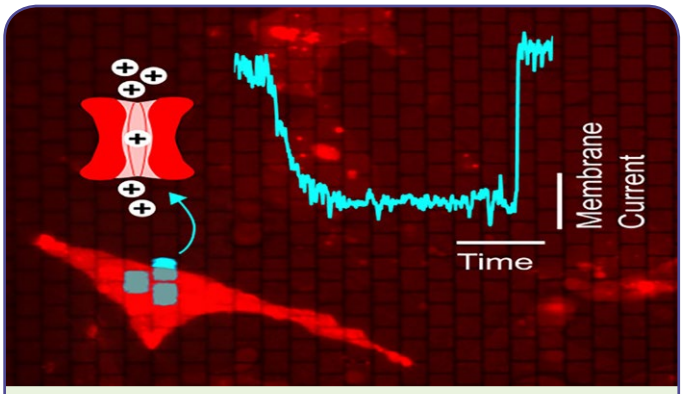
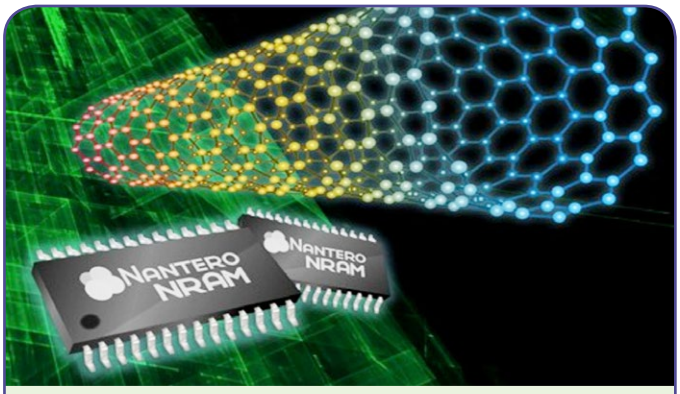
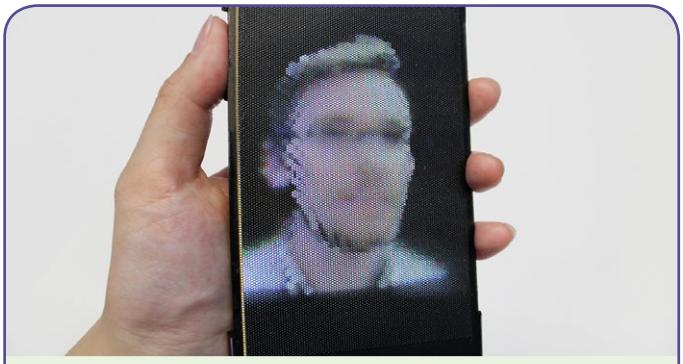
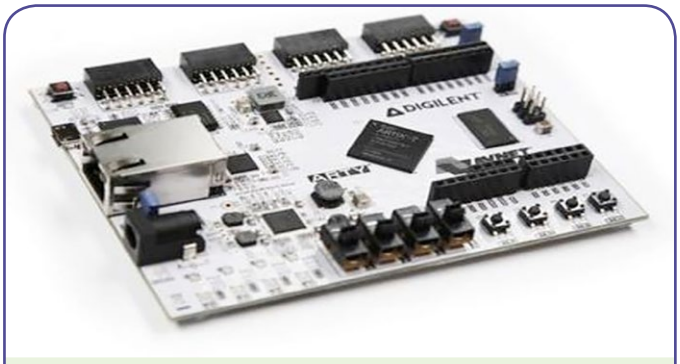
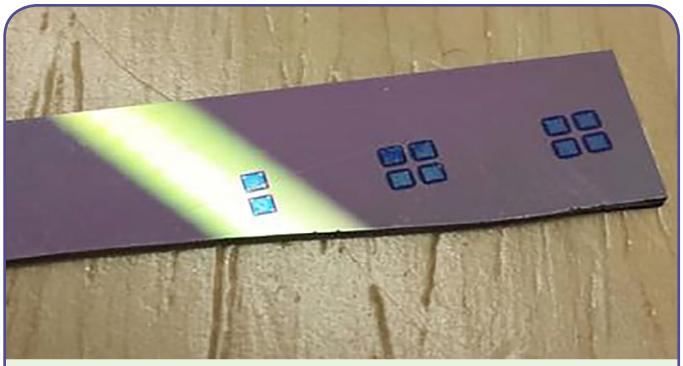










Toward OLED-controlled live neural networks

By Julien Happich

In a paper titled "Arrays of microscopic organic LEDs for high-resolution optogenetics" published in the Advance Sciences journal, scientists at the University of St Andrews detail how they leverage very fine pixel pitch OLEDs in place of a Petri dish to individually trigger living cells and observe their electric activity.

Working with Dr Gareth Miles from the School of Psychology and Neuroscience, Professor Gather and his team used OLEDs as a substrate to manipulate individual, live cells from a human embryonic kidney cell line that were tweaked to produce a light-sensitive protein.

Upon exposure to blue OLED light from pixels directly underneath the cell, the researchers stimulated the electric activity of individual targeted cells, while neighbouring cells remained in the dark and stayed inactive.

The real first here, was that the researchers used a 20mm^2 OLED microarray (from Fraunhofer FEP, based on a CMOS backplane featuring 230,000 individually addressable pixels) with 6×9µm^2 pixels, smaller than the actual cells under study. This enabled the team to optically stimulate not only discrete cells but also different parts of a given cell.

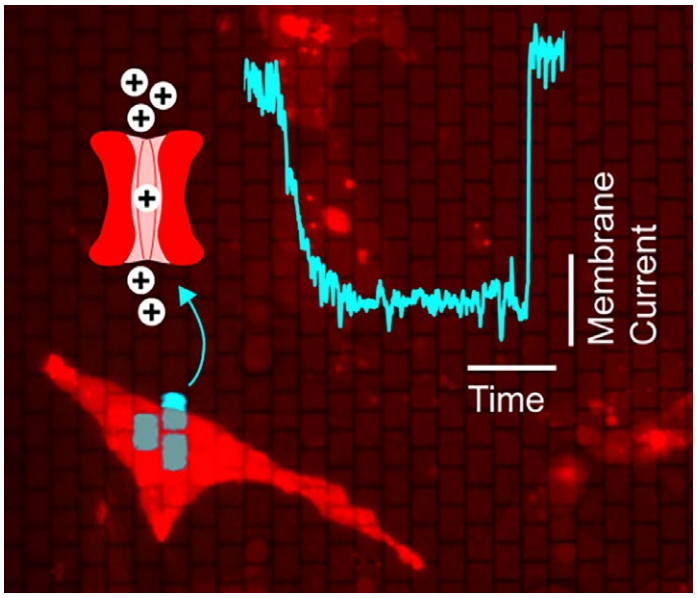
To ensure the shortest optical path (from the OLED pixels used as a substrate) to the cells under study while protecting the OLED active layers, the team only applied a 1.5µm thin-film encapsulation barrier (three layers of Al_2O_3 and two layers of polymer), which they had reported, was enough to keep the OLED functional over several days without noticeable degradation even when fully immersed into a salt buffer solution.

The microarray was then bonded to a flexible flat cable that connects to a custom HDMI driver interface.

In their experimental setup, the team used a standard cell line to test their approach, with a micro-electrode placed manually to collect the electric response from a given cell. By lighting discrete OLED pixels underneath the modified photo-switchable cells, the researchers were able to switch the cell's membrane potential conductivity states, testing different ion channel activation and deactivation kinetics.

Depending on the cells used, these ranged from 1ms for activation and 21ms for deactivation to bi-stable switching characteristics (the conductive channel being opened or closed by different wavelength exposures). In fact, the emission spectrum of the OLEDs was tuned to match the spectral response of the cells under study.

Probing dozens or even thousands of cells in parallel would quickly become tedious if only relying on individually placed electrodes, recognized Gather in an interview with EETimes Europe, but the professor regarded this OLED-based experiment as only a first step.



"The next step would be to laminate optical or electrical sensors so that when actuator cells start to fire, we could detect the cells' response and interactions across full networks" he said, hinting at the study of neuronal networks.

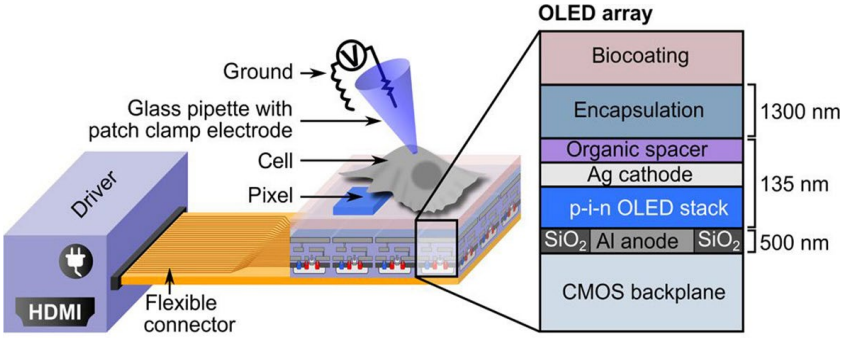
"As soon as you can have a parallel readout, you can probe one cell and see how it can be excited by other cells".

In fact, not only this OLED-approach could be used to study neural networks, it could even be used to actively tweak such networks, playing on different ion channel activation and deactivation kinetics.

"Rather than having a probe on one neuron, with mechanically flexible micro-OLEDs, you could envisage bio-implants in real brains, wrapped around the surface of the brain", Gather said, adding that with a closed loop and learning algorithms, you could probe parts of the brain and try to correlate all firing actions, advancing knowledge of the neuronal dysfunction that underlies devastating neurodegenerative conditions such as Alzheimer's Disease, Parkinson's Disease and Motor Neurone Disease.

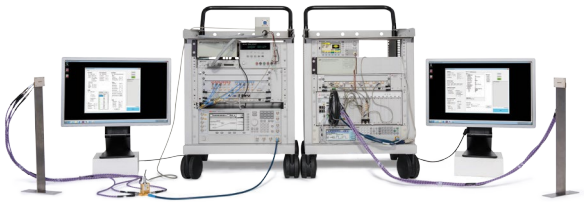
Today, such studies are performed with bulkier micro-electrodes.

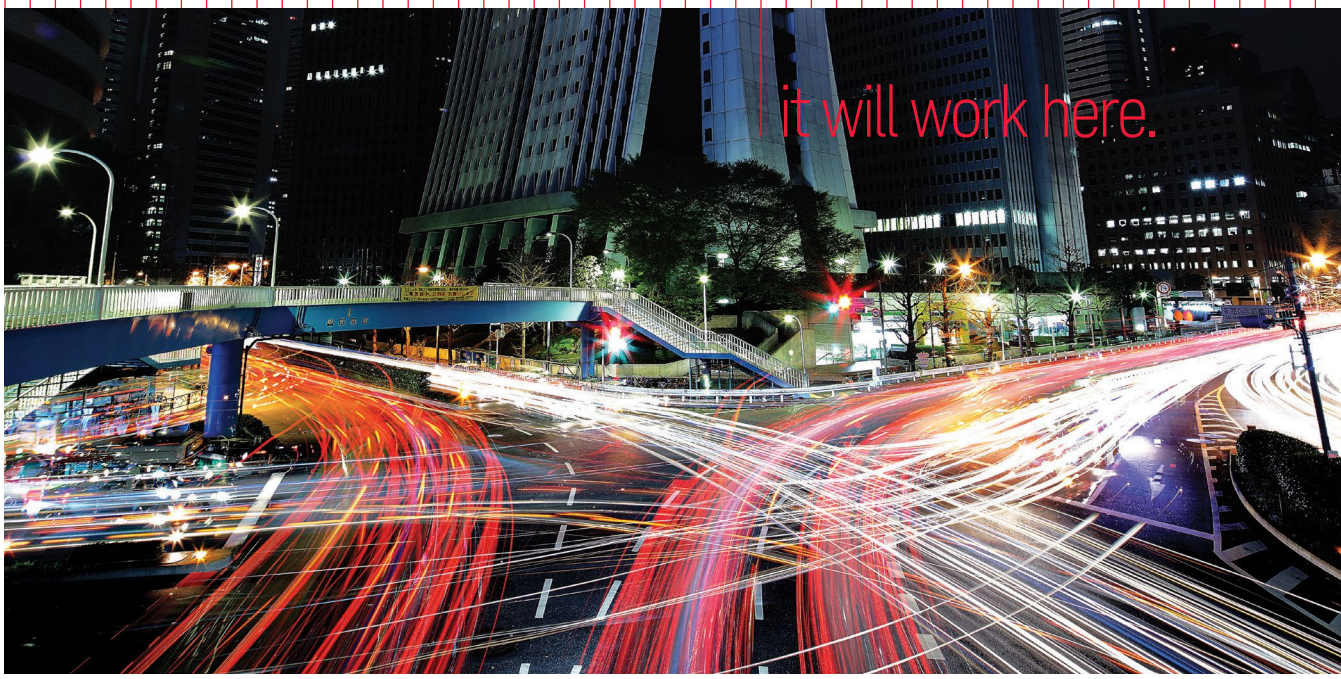
"Ultimately, you could dynamically control parts of the brain, say to silence the parts that are causing an epileptic seizure", Gather concluded.



The OLED microarray with cells adhered on top of the array (not drawn to scale). The microarray is connected to a high-definition multimedia interface (HDMI) driver with a flexible connector. Each pixel of the array can be turned on and off by the driver and the CMOS backplane. Light-induced changes in cell membrane current are measured with a patch clamp electrode (voltage clamp mode, whole-cell configuration). The cross section on the right shows the layer structure of the OLED array.

If your 5G idea works here...





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Globalfoundries at work on next-gen FDSOI process

By Peter Clarke

The 22FDX fully-depleted silicon-on-insulator (FDSOI) process developed by Globalfoundries Inc. (Santa Clara, Calif.) is on track to debut later this year and the company is working on the follow-on process, according to chief technology officer Gary Patton.

Globalfoundries claims its 22FDX platform, four processes with different optimizations, can deliver FinFET performance and energy efficiency at a cost comparable with planar 28nm CMOS. The ability to perform back-biasing provides the opportunity to dynamically change the operation of transistors from performance to minimal leakage.

However, FinFET production remains the mainstream option for leading edge ICs that is best supported by foundries, including Globalfoundries, and by IP developers. In addition Samsung's foundry is also offering a 28nm FDSOI process.

Patton, previously a career-long IBM researcher, was brought in to Globalfoundries when the foundry acquired IBM's semiconductor operations.

"We looked at both FinFET and FDSOI is perfectly suited for the mobile space," Patton told EE Times Europe on the sidelines of the IMEC Technology Forum held in Brussels this week. "The work started in Malta (New York) and has transferred to Dresden. The yields are ahead of schedule and the focus is on getting design IP built up."

Globalfoundries is working with a company called Invecas Inc. to develop foundation IP for its 14nm FinFET and 22nm FDSOI manufacturing processes. The schedule for 22FDX has Globalfoundries starting risk production for customers late in 2016 with volume manufacturing arriving in 2017.

Patton made the point that FinFET processes with their high drive current capability are well suited to driving signal lines across large chips and where sustained performance is required. However, for smaller chips and chips where power consumption is key then FDSOI is a better option. Patton also makes the point that FinFETs have a quantized drive regime where a developer must choose between 1, 2 or more fins, which is not suited to analog or RF signal.

But although Globalfoundries has been extolling the virtues of 22FDX for analog and the RF in the Internet of Things (IoT) Patton makes the point that the process also addresses digital requirements. "There's a ton of digital business in mobile sitting at 65nm, 40nm. And the cost of migrating that to FinFET is high compared with moving to another planar process, such as FDSOI," he said.

However the FDSOI process – originally research by IBM and then championed by STMicroelectronics and now Globalfoundries and Samsung – has had a difficult gestation. It is four years since an initial deal between STMicroelectronics and Globalfoundries to produce FDSOI in volume at the Dresden wafer fab.

With the possibility of potential design wins for FDSOI going to 16nm and 10nm FinFET processes a lack of road-map could be seen as a disadvantage. Modern design involves the migration of larges amounts of proprietary and third-party IP cores and therefore continuity of process is significant.

"We have a next generation fully depleted process that is underway in Malta," Patton said without confirming a nominal node name. The labelling of nodes with a minimum dimension is largely moot in the modern era. Upcoming 10nm and 7nm nodes from TSMC will have minimum feature sizes of about 20 and 14nm respectively and be produced on 32nm or 36nm pitch.

FDSOI is driving ST's automotive businesses

By Peter Clarke

The fully-depleted silicon-on-insulator (FDSOI) chip manufacturing process championed by STMicroelectronics has become almost the default choice for digital manufacturing within the automotive and discrete group (ADG) business unit at ST, according that group's senior executive.

And that emphasis on FDSOI will continue through the manufacture of automotive microcontrollers in 28nm FDSOI, said Marco Monti executive vice president responsible for the ADG business unit.

Monti said that while ST's most advanced microcontrollers are on 40nm CMOS the next generation will be on 28nm FDSOI with some sort of non-volatile memory possibly based on phase-change memory. "The use of FDSOI in MCUs at ST is driven by automotive," said Monti. Rival European chip company and automotive supplier NXP Semiconductors is also expected to develop MCUs based on 28nm FDSOI.

One particular automotive IC development – Mobileye's EyeQ5 – is not targeting FDSOI, but this is because it is a very long-term and high performance project that will be unlikely to see silicon before the end of the decade, Monti told *EE Times Europe*. In the near- to medium-term, with digital electronics in automotive applications growing rapidly, FDSOI is key to ST's strategy, he said.

"EyeQ5 is a very long term development and very complex; for full level-4 autonomous driving. It will reach production in 2022 and volume in 2025 but all the rest in ST automotive is driven by FDSOI technology. The EyeQ4 vision processor that will enter production in 2017 is on FDSOI. That is targeting level-2/level-3 autonomy," said Monti. The development team at ST has just won a special award from customer Mobileye because the EyeQ4 reached higher-than-expected performance levels, Monti added.

There are numerous other examples of FDSOI chips in development, Monti said.

These include: a next-generation Sirius XM satellite radio chip in 28nm FDSOI that will sample this year; ST's car-communications activity with Israeli customer Autotalks Ltd. "Automotive-grade Wi-Fi is on 28nm FDSOI; all the processors for automotive entertainment are going on FDSOI, our telematics processor. And we have a specialization in 28nm FDSOI for RF to make 77GHz radar for ADAS applications," Monti added.

"FDSOI is not just a manufacturing node for us. It's a whole cluster of technologies for all things in the car."

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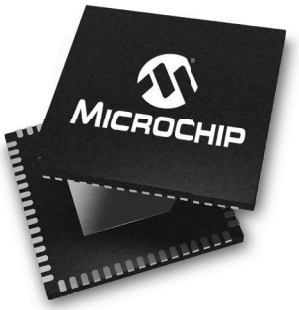

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Google designing AI processors

By Rick Merritt

Google has developed its own accelerator chips for artificial intelligence it calls tensor processing units (TPUs) after the open source TensorFlow algorithms it released last year. The news was the big surprise saved for the end of a two-hour keynote at the search giant's annual Google IO event in the heart of Silicon Valley.

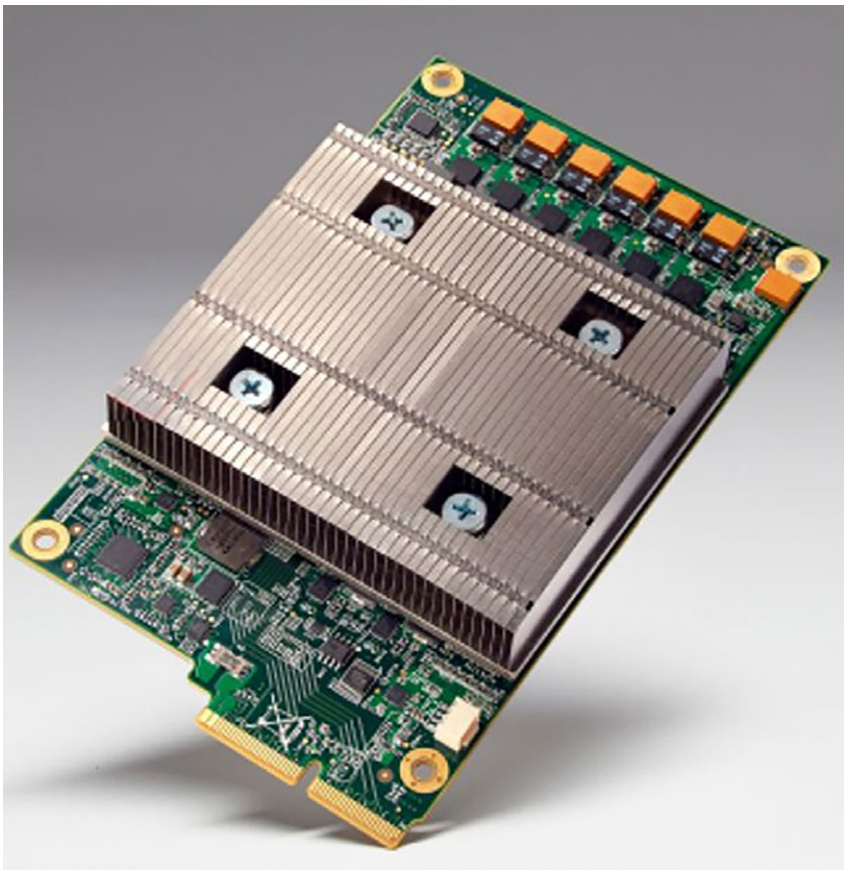
"We have started building tensor processing units…TPUs are an order of magnitude higher performance per Watt than commercial FPGAs and GPUs, they powered the AlphaGo system," said Sundar Pichai, Google's chief executive, citing the Google computer that beat a human Go champion.

The accelerators have been running in Google's data centers for more than a year, according to a blog by Norm Jouppi, a distinguished hardware engineer at Google. "TPUs already power many applications at Google, including RankBrain, used to improve the relevancy of search results and Street View, to improve the accuracy and quality of our maps and navigation," he said.

The chips ride a module that plugs into a hard drive slot on server racks. Engineers had them running just 22 days after they tested first silicon said Jouppi, who previously helped design servers and processors at Hewlett Packard and Digital Equipment.

Given the nature of AI algorithms, "the chip [can] be more tolerant of reduced computational precision, which means it requires fewer transistors per operation…[and thus] can squeeze [in] more operations per second," he said.

The project started several years ago. Google has been hiring engineers with semiconductor expertise for some time. However, it managed to keep secret what they were working on, despite the fact the chips are already running in systems.



The TPU fits on a module that plugs into a hard disk slot in a server rack. (Image: Google)

The company is not the first to design an accelerator specifically for AI. Nervana Systems is preparing a cloud service that will be based on its own AI accelerators. Movidius has its own merchant chip for embedded applications, and recently announced plans for a high-end version.

The news comes amid a broad debate in the computing industry over the last few years about how best to accelerate emerging AI algorithms such as convolutional neural networks. To date, Microsoft and Baidu have opted to use FPGA accelerators for their cloud services. Facebook designed a GPU accelerator and made it open source.

The algorithms caught fire when they showed about three years ago the ability to recognize images as well or better than humans. Google's demonstration at playing Go was another key milestone given the complexity of the game.

In one game of the match, "move 37 was the most beautiful move due to its creativity," said Pichai. "We normally don't associate computers with making creative choices, so this is a significant achievement in AI, he said, noting the human Go champion has since used the move in other games.

Google released no details about the new chips. Pichai said the the search giant's TensorFlow algorithms which he said has one become of the most popular projects on GitHub.

Don't expect Google to provide merchant versions of the chips. Access to TPU hardware "will be one of biggest differentiators for the Google Cloud Platform," he added.

Pichai gave examples of how Google is using AI to make robotic arms more accurate. It is also working on an expert system to help prevent diabetic blindness through early diagnosis.

"We live in an extraordinary period for computing…The real test is whether humans can achieve more with AI assisting them so things previously thought impossible may become possible," he concluded.

Google claimed the TPUs are three process generations ahead of the competition, said Kevin Krewell, senior analyst with Tirias Research. "The TPUs are "likely optimized for a specific math precision possibly 16-bit floating point or even lower precision integer math," Krewell said.

"It seems the TPU is focused on the inference part of CNN and not the training side," Krewell said. "Inference only requires less complex math and it appears Google has optimized that part of the equation.

"On the training side, the requirements include very larger data sets which the TPU may not be optimized for. In this regard, Nvidia's Pascal/P100 may still be an appealing product for Google," he added.

Google Home is a voice-activated assistant coming this fall, similar to Amazon's Echo. (Image: EE Times)

Beyond the surprise news of the TPUs, the annual Google IO was in many ways about the search giant playing catch up with rivals Amazon, Apple and Facebook's Oculus in areas from virtual reality to smart homes and watches.

In VR, Google will make its own hardware, and has announced a reference design for VR headsets and controllers others cane make using extensions in Android N. A beta version of the operating system is available now with the first VR hardware using it coming in the fall.

Google calls its approach to VR Daydream and worked with handset and chip vendors to define a specification for smartphones that are Daydream-ready. Phones compliant with the spec are expected this fall from the likes of HTC, Huawei, LG, Samsung and Xiaomi.

Android N will support VR latencies as low as 20 milliseconds, Google claimed. The company is working with game and movie developers to release VR titles for Android N. It will also support Daydream VR in its own services including new and existing YouTube videos, Google Photos and Street View in Google Maps.

Overall, Android N will pack 250 new features, including support for Vulkan, the graphics API also used by desktops and game consoles. It sports file-based encryption, and a faster runtime and new JIT compiler to load apps faster while using less memory.

Separately, Google announced it will ship this fall its own voice-based controller called Home, competing with the Amazon Echo. Home will act as a gateway controlling delivery of digital music and video to speakers and TVs. It has its own built-in speakers, links to home devices like Nest thermostats and can process natural language Google search requests.

In addition, Google announced Android Wear 2.0, a version that better mixes and matches data from various applications and is ready for cellular-enabled watches.

Finally, Google also previewed Duo, its answer to Apple's FaceTime video calling app. It uses features in the WebRTC standard to show video of a caller before a user picks up a call and will be available on both Android and iOS this summer.

European battery 'Gigafactory' opens

By Graham Prophet

BMZ GmbH (Karlstein-Großwelzheim, Germany) has opened the first section of what will be Europe's biggest lithium-ion battery factory, labelling it as "Europe's Gigafactory" in an allusion to the Tesla battery plant being built in the western USA). Over the next four years, BMZ plans to more than quadruple production areas in Germany.

With construction taking only a little over a year, BMZ, a developer and producer of intelligent lithium-ion batteries, has now opened up the first two production, logistics and office buildings in addition to an existing production areas of 7,000 m² at the company's present headquarters. In the manufacturing units comprising 4,800 m² each, up to 200 million lithium-ion batteries of the most different kind and size with an overall storage capacity of about 15 GWh can be developed, produced and tested every year.

By 2020 four further production, laboratory and office buildings covering a total space of 15,000 m² are planned on the new company site of 55,000 m². After the completion of the construction works up to 1,500 BMZ employees will produce 800 million lithium-ion batteries in a range of different sizes annually with an overall storage capacity of 30GWh, from the industrial site in Karlst ein-Großwelzheim alone.

At present the company has around 120,000 m² production sites in its own companies in Germany, China, the USA and Poland. Company founder and owner Sven Bauer explains, "The current discussions on subsidies for electric cars often forget that lithium-ion batteries are also used in e-bikes, electrical appliances, gardening tools, energy storage systems, transport vehicles, excavators and so on."

"Unlike electric cars we are presently undergoing a real demand boom in many of these sectors, and we assume that the demand in these segments will further increase by 15 to 30% annually in the coming years depending on application range. The modular concept of our new ultra-modern factory units enables BMZ to respond even faster and more flexible to this growth scenario as well as specified customer requests in the future."

The setup of Europe's biggest lithium-ion battery factory in Karlstein shows – according to Bauer – how important this technology has become especially for the industry location Germany. The battery expert assumes that by 2020 wireless solutions will dominate the markets; a development that will offer enormous growth opportunities.

The request for maximum mobility stimulates not only the demand for well-known appliances such as vacuum cleaners or drill hammers. With modern lithium-ion batteries numerous new ideas can be realized of which robotic lawn mowers are only one of many examples. The market potential for battery-powered appliances is enormous.

"From our point of view it is most important to commonly build up our own production of lithium-ion cells in Germany, too. That is the only way to reduce the dependency risks on the few, mainly Asiatic cell producers in the long run," says Bauer.

As a first intermediate step, BMZ intends to launch their own extremely efficient cell, which is to be applied in their own as well as customer-related battery systems. The cell, which will be available in prototype form at the end of this year claims 100% higher durability, 68% more performance, 88% more energy, 400% more charging current and up to 60% more capacity compared with usual cells according to the industrial standard 18650.

In 2015, the company, which was founded in 1994, achieved a turnover of some 350 million euros as the largest independent European lithium-ion battery system developer and manufacturer, with more than 1,200 employees worldwide. The 500 million threshold is expected to be broken in 2020 at the latest.

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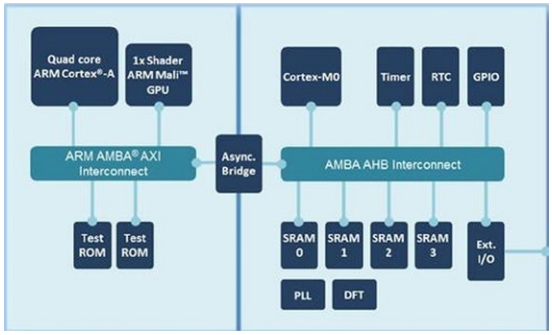
ARM describes 10nm test chip

By Jessica Lipsky

ARM announced it taped out a 10nm FinFET test chip in January at TSMC. Chips made in the process will be in handsets by the end of the year, ARM said, descri-bing the node as relatively expensive and focused on lowering power.

The ARM test chip used four of its yet-to-be-disclosed
Artemis cores running at 2.8 GHz, an unknown GPU and memory subsystem among other components. Unlike previous nodes, the TSMC 10nm process is focused less on pushing performance to the max and more on lowering power consumption, ARM said.



Test chip architecture Source: ARM

Compared with a Cortex A-72 on TSMC's 16FF+ process, the 10nm SoC operating on the same frequency showed a 0.7%, 11% and 12% improvement in performance depending on the use of overdrive which ARM defines as nominal + 100mV. Eventually, 10nm chips should show a 30% improvement in power consumption compared with its predecessors.

The Artemis core itself appears to be focused mainly on lowering power consumption and size based on ARM's comments about the test chip.

"Artemis is a small core, so you're going to get some architectural benefits in leakage, just as much frequency, better power and smaller," said Ron Moore, vice president of marketing for ARM's physical design group.

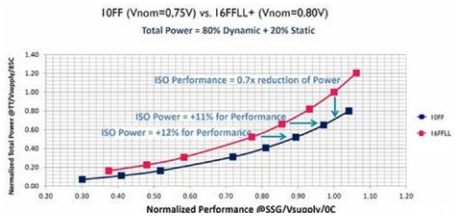
"Performance between Artemis and an A-72 are going to be pretty much at the same level."

TSMC has been working closely with ARM on process technology and IP for the past four years. However, ARM also is working with Samsung as its foundry aggressively pushes toward its own 10nm FinFET process.

While Samsung and TSMC race to be the first to market with a 10nm node, Moore isn't concerned about who comes in first. "The fin size is different but I can accomplish the same thing using Artemis in both processes," he told EE Times.

Jim McGregor, Tirias Research principal analyst, expects Samsung and TSMC to continue to battle it out but also run into some of the same challenges Intel faced when ramping 14nm.

"Both these guys are ramping aggressively with ARM-based products. That really shows the strength of the ARM architecture," McGregor told EE Times. "If you had to compare process to process, when Intel gets to 10nm they'll probably still have the most aggressive process of any of them, but Intel hasn't shown their ability to be an effective foundry," he said.



Data on total power versus performance of 10nm FinFET test chips compared to 16nm FinFET. Source: ARM

Moving to the 10nm node comes with additional costs. Moore said the design cost for developing a physical implementation of 28nm was about $5.5 million, while 10nm will cost approximately $32.5 million - a figure initially given by International Business Strategies in August 2015. A 10nm chip requires more iterations, IP, and likely more machine time – all of which is likely to trickle down as additional costs for chip designers and their foundries, he said.

"The early ones in pay for the early development cost. They pay for the high really expensive design tools, they pay the big premiums because they can afford more and because their markets are bigger," said VLSI Research CEO G. Dan Hutcheson. "I think the cost-to-design argument, to some extent, is a bragging right."

Hutcheson continued that the general design cost for a chip shouldn't be more than 15% of its sale price, and added that there is a lot of complexity in that design figure. The amount of IP in the ecosystem, the cost of a design team, the capability of design tools and the size of the market all play into that $32 million figure – which will shrink as 10nm proliferates.

At an analyst event, ARM didn't provide updates on a lower-cost alternative, fully-depleted silicon on insulator (FD-SOI), which the company acknowledged as a viable technology during the FD-SOI Symposium last month.

"FD-SOI is still very much a good technology and it is a very power efficient technology," Moore said.

"We do not see the customer adoption and the ecosystem. What you're missing is the LPDDRs, the memory interfaces, the IP kind of stuff," he said. "FD-SOI is probably not being adopted as well as it could because the ecosystem is trailing. I think the foundries that want to do the FD-SOI will have to invest," he added.

One of the challenges of FD-SOI adoption is the analog, RF and high speed interface IP needed to support diverse market segments, Moore told EE Times, pointing to the needs in mobile, enterprise, and embedded/IoT markets.

ARM already ports devices to FD-SOI, Hutchenson noted, though the porting process is tedious. The issue isn't the ARM core but supporting a variety of ecosystems and thousands of potential IP. Moore said foundries will need to provide "seed funding" to build out the IP ecosystem for each of market, including porting complex IP from BULK to FD-SOI.

Kelvin Low, Samsung's senior director of foundry marketing, said his company has "substantial IPs" for FD-SOI that have been product tested. A GlobalFoundries' representative said the company will support FD-SOI for SoCs by the second half of 2017.

"We are developing IP [on our 22FDX platform] concurrently with technology development," a GlobalFoundries spokesman said.

"Some of them have gone through early silicon validation and others are in various stages of design and silicon validation," he said. "Prototype SoCs are being taped out now using early versions of IPs. A complete set of silicon validated foundation and complex IPs will be available for SoC design start and tapeout, [and] we are on target to support SoC product launch in 2H2017," he added.

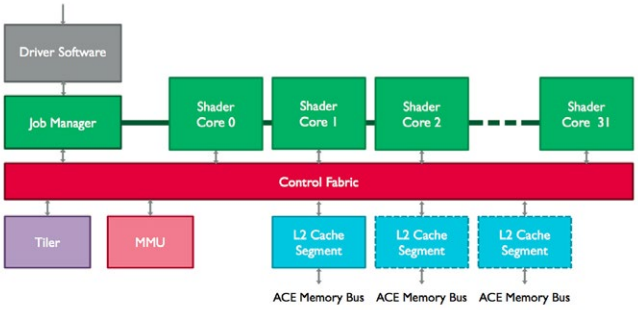
"No company has the breadth of the entire ecosystem of IP," Hutcheson told EE Times. "If I were to guess, it's in their advantage to minimize the number of ecosystems they have to support."

ARM's Bifrost steps up graphics, bridges to machine learning

By Peter Clarke

The Mali-G71 GPU core is ARM's first that follows a new architecture called Bifrost that has been launched providing support for the Vulkan API from the industry-run Khronos Group.

The architecture includes maths capabilities that could be used by other software as part of a heterogeneous system architecture. That could include neural network software but ARM executives stressed that Bifrost is first and foremost an architecture for raster, tile-based graphics processing units (GPUs).



Top level architecture of Bifrost showing up to 32 universal shader cores, Source ARM.

The previous architecture – Midgard – is the one that underlies ARM's T-series Mali GPUs and has up to 16 unified shader cores and SIMD [single-instruction multiple data] instruction set architecture. Bifrost supports up to 32 unified shader cores with a scalar ISA, full hardware cache coherency and something called clause execution.

The primary goal, according to Sean Ellis, GPU architect with ARM, was to achieve more performance per square millimetre of silicon and per line of "real-world" shader code. And this has been achieved to tune of about 50 percent through the use of a new scalar, clause-based ISA, with quad-based arithmetic units

Whereas Midgard GPUs use SIMD vectorization Bifrost GPUs will use quad vectorization in which four scalar threads from a 2 by 2 pixel are executed in lock step. Each thread fills one 32-bit lane of the hardware and four threads doing a vec3 FP32 add takes three cycles. In short quad-vectorization is compiler friendly and improves resource utilization.

Clause execution is another refinement that is used to reduce overhead compared with the previous graphics architecture. A "clause" is defined as a sequence of instructions that are self-dependent and without variable latency. Whereas previously temporary registers are used after every instruction under Bifrost an architecturally visible state through temporary registers is only guaranteed after each clause. The back-to-back execution of instructions within a clause allows for aggressive optimization and saves power. Clause boundaries are decided in the compiler, Ellis told journalists and analysts.

When asked if there was specific support within Bifrost for GPU-computing – where the GPU is used to run software to which it may be better suited than the CPU core cluster – ARM executives said that decisions had been taken to include support for a variety of data types that are not generally used in graphics. These include 8, 16 and 32bit integers as well as 16-bit floating point.

The FP16 can be used for some pixel shaders at twice the nominal throughput. Similarly Bifrost supports 64bit floating-point precision at half nominal throughput. Meanwhile the integer math and FP16 are useful for deep learning applications, Ellis said.

ARM has never been particularly keen on the raytracing approach to graphics rendering, which is a completely different approach to tile-based rendering. Indeed it acquired Geomerics Ltd. in 2013, a leader in software engines for lighting effects in software games. Ellis told *EE Times Europe*: "Ray tracing is not explicitly excluded [from Bifrost]. But we can do lighting, shadowing, glare effects in other ways."

Vulkan

Vulkan is a 3D graphics API for the next 20 years, said Jem Davies, ARM Fellow and vice president of technology for media processing. "Vulkan 1.0 was released in February with unprecedented support. It is available on the desktop in Windows and Linux and will be supported in upcoming N generation of the Android operating system.

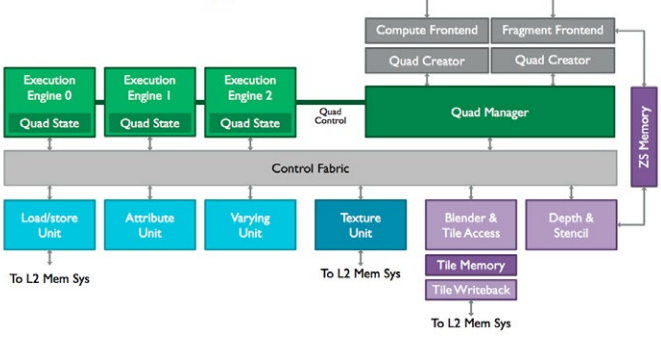
"In 2014 the traditional 3D APIs were in trouble with unpredictable performance and the emergence of proprietary efforts such as Mantle, DX12." So a crash effort in a next-generation OpenGL initiative was launched. AMD donated its Mantle technology.

The major result is that under Vulkan more responsibility is given to the application making for a lower overhead driver. The driver handles memory allocation, resources, and thread management to generate command buffers. Vulkan is multithread and multicore friendly and error checking is opt-in, said Davies. "Vulkan is a great fit for mobile graphics architectures because there is no wasted effort trying to look like a desktop GPU," he added.

ARM already has Vulkan drivers for T880/T860/T760 and the Mali-G71 driver is ready and awaiting silicon.

And progress continues with Vulkan 1.1 expected soon, said Davies. "I think we will see features added to further reduce power and bandwidth. Thermal throttling of processors is a big deal." Davies said that texture compression helps in this regard and AFBC [ARM Frame Buffer Compression] is becoming commonly supported but when asked if AFBC would be standardized within Vulkan 1.1 said: "We would welcome AFBC being established as standard but it's unlikely."

However, Vulkan 1.1 could also include further developments to support GPU-compute. "The GPU-compute voice is getting louder as time goes on," Davies said.



Inside the shader core showing quad-thread fragment management and execution engines. Source: ARM.

'Internet of Sensors' project kicks off in Europe

By Peter Clarke

IoSense, a European pilot line project has kicked off in Dresden, Germany at the site of project leader Infineon Technologies AG.

IoSense is a three-year project with 33 partners from six countries collaborating on R&D across the value chain for sensors and a budget of €65 million (about $70 million). Although there are numerous academic and research institute partners the main commercial participants are Infineon, AMS, Philips Lighting and Siemens.

The European Commission is providing €14.7 million (about $16.5 million) and the German state of Saxony and the German Federal Ministry of Education and Research (BMBF) will contribute €5.2 million (about $5.8 million). The name derives from Internet of Sensors and is intended to support the creation of three pilot lines (two front-end and one back-end) for the production of both discrete and integrated sensor systems.

The project has been divided into 7 technical work packages with a further two focused on the management of the project and standardization and dissemination of the results.

"Sensor solutions from Infineon in cars make a major contribution to improving road safety," said Reinhard Ploss, CEO of Infineon, in a statement. "With an increasingly networked world and the Internet of Things, the demand for such sensor solutions will see a dramatic rise. In addition, sensors are increasingly employed in smartphones and lifestyle products. We will benefit from this market growth through new sensor technologies and competitive production methods."

Infineon Technologies Austria AG is set to lead another European research project that will begin this month. Semi40 will focus on manufacturing power semiconductors according to Industry 4.0 requirements.

Machine-learning radars may be coming to automotive

By Peter Clarke

The IMEC research institute (Heverlee, Belgium) plans to make future sensors, and specifically radar sensors, devices that extract useful information locally and even become learning machines.

IMEC is already working with automotive radar market leader Infineon Technologies AG at 79GHz in 28nm CMOS. Now it wants to go to a yet smaller wavelength and add machine learning to the back end of its sensors said Wim van Thillo, program director for perceptive systems at IMEC, speaking at the IMEC Technology Forum.

Van Thillo said his group is already working on a 140GHz chip. At this frequency the wavelength is 2.2mm and his group is aiming for more than 4GHz of bandwidth from a chip measuring 1 square millimeter, he added.

The advantages will include higher distance and angular resolution at lower power in a much smaller system size with the radar able to include the antenna-on-chip. In addition to angle and distance the radar is able to provide speed information via a mini-doppler effect. The use of multiple antennas integrated on to the chip will result in enhanced Doppler resolution and a better depth resolution.

The signal processing that will be needed to extract speed information is likely to be taken further with the use of algorithms for pattern recognition and automatic learning. As a result Van Thillo envisages a time when the radar will be able to recognize and distinguish the signature of pedestrians, bicycles and cars from their mini-Doppler signatures.

Massimiliano Maranella, program manager for millimeter-wave perceptive systems, said that 28nm CMOS is being used again and that in simulation at least the signals look good enough to use. However, it acknowledged that a 28nm CMOS platform would not be suitable for long-range (300m) automotive radar.

A complication is that the plastics used in bumpers and metallic paints tend to absorb the energy at 140GHz, Maranella said.

However, while the frequency may be used in shorter-range gesture recognizing systems the learning can be extended across a broader set of perceptive systems including automotive.

For example, such machine learning radars will be part of a sensor fusion system that combines visible and radar to make the best identification. But one of the big advantages of the coming connected-car is that vehicles will be able to benefit from "fleet-learning" Van Thillo said. So cars will be learning how to identify and react to hazards far faster than an individual vehicle would.

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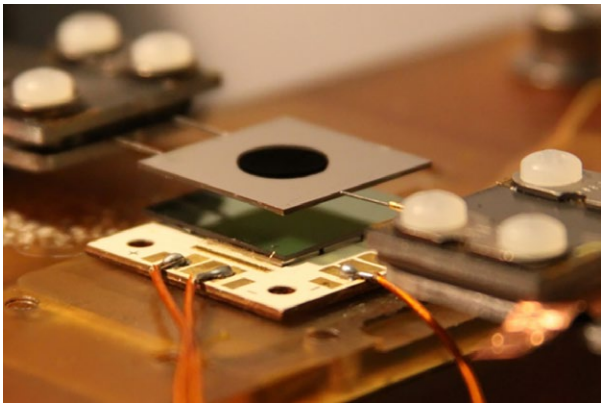
CNTs & photonics to break solar conversion theoretical limits

By Julien Happich

In their Nature Energy paper "Enhanced photovoltaic energy conversion using thermally based spectral shaping", MIT researchers demonstrate how they were able to boost a traditional photovoltaic cell conversion efficiency by converting the broadband sunlight to a narrow-band thermal radiation precisely tuned for the photovoltaic cell at hand.

Relying on the broadband absorption of vertically grown carbon nanotubes (CNTs) integrated with a one-dimensional photonic crystal selective emitter and paired with a tandem plasma–interference optical filter, the researchers managed to suppress 80% of unconvertible photons, achieving a solar-to-electrical conversion rate that exceeded the performance of the photovoltaic cell alone.



MIT's thermophotovoltaic assembly showing a circular layer of ultra-black CNTs covering a one-dimensional photonic crystal, over an optical filter (green) cover the standard solar cell. Courtesy, MIT's researchers.

Their research also established that the resulting device could operate more efficiently while reducing the heat generation rates in the photovoltaic cell by a factor of two for a given output power density.

With solar thermophotovoltaics, lead author MIT doctoral student David Bierman sees a new energy harvesting route that could help traditional solar cells break their energy conversion theoretical limits.

Instead of dissipating unusable solar energy as heat in the solar cell, thermophotovoltaics devices first absorb all of the energy and heat through an intermediate component (the ultra-black CNT layer on top of a one-dimensional photonic crystal seen on the top of the thermophotovoltaic assembly).

Reaching high temperatures (1,000 degrees Celsius in their experiment), these added layers are tuned to only emit thermal radiation at the optimal wavelengths of light for the solar cell to operate at peak efficiency.

By pairing conventional solar cells with these custom-designed emissive layers, one could more than double the theoretical limit of efficiency, potentially making it possible to deliver twice as much power from a given area of panels, expects Bierman.

One implementation could be to use a conventional solar-concentrating system, with lenses or mirrors that focus the sunlight, to maintain the high temperature.

An advanced optical filter would let through all the desired wavelengths of light to the PV cell, while reflecting back any unwanted wavelengths. Those reflected wavelengths would then get re-absorbed, helping to maintain the heat of the photonic crystal.

Because the photonic device produces emissions based on heat rather than light, such a thermophotovoltaic device would be unaffected by brief changes in the environment, such as clouds passing in front of the sun, as the researchers demonstrated.

It could even be coupled with a thermal storage system to make use of solar power on an around-the-clock basis. In addition, because of the way the system harnesses energy that would otherwise be wasted as heat, it can reduce excessive heat generation that can damage some solar-concentrating systems.

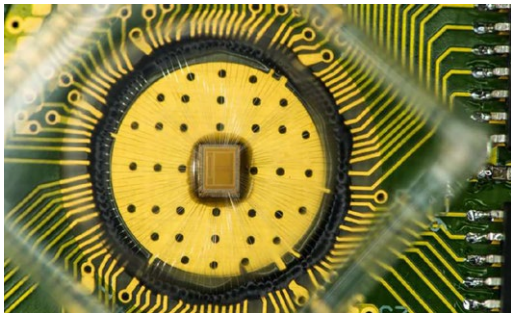
The researchers are now looking at implementing larger versions of their small, laboratory-scale experimental unit, trying to find new ways of manufacturing such systems economically.

3-bits per cell for IBM's phase-change memory

By Julien Happich

Five years after they had published their first results proving the viability of a 2-bit per cell phase-change memory (PCM), scientists at IBM Research have managed to push their coding scheme and design to store 3 bits of data per cell.

The researchers first demonstrated reliable storage and moderate data retention of 2 bits/cell PCM, on a 64 k cell array, from room temperature (around 30°C) to 80°C and after 1 million SET/RESET endurance cycles. Under similar operating conditions, they then demonstrated the feasibility of 3 bits/cell PCM (eight levels of data encoding), with a chip consisting of a 2×2 Mcell array with a 4-bank interleaved architecture.



The memory array size is 2×1000µm×800µm and the PCM cells are based on doped-chalcogenide alloy, they were integrated into the prototype chip serving as a characterization vehicle in 90nm CMOS baseline technology.

"Reaching three bits per cell is a significant milestone because at this density the cost of PCM will be significantly less than DRAM and closer to flash", said Dr. Haris Pozidis, manager of non-volatile memory research at IBM Research and one of the authors of the paper presented at the IEEE International Memory Workshop in Paris.

The multi-bit storage capability relies on a set of drift-immune cell-state metrics and drift-tolerant coding and detection schemes.

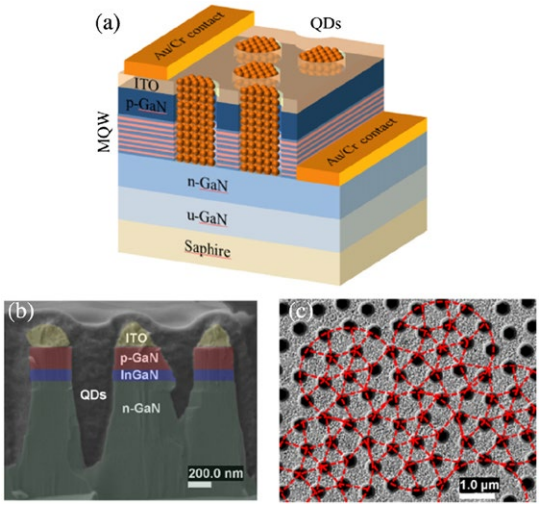
Quantum dots get deeper into LEDs

By Julien Happich

Boasting record-breaking colour conversion effective quantum yields, an international team of researchers has designed a novel photonic quasi-crystal LED structure which deeply embeds quantum dots within the whole stack of the LED's active layers.

The researchers first grew a LED stack of GaN/InGaN Multi-Quantum Well onto a sapphire substrate, and then used nano-imprint lithography and plasma etching to "punch" the whole stack and structure it as a 12-fold symmetric quasi-crystal (PQC).

Forming an array of 480nm radius cylindrical holes with a lattice pitch of 750nm, the PQC structure was etched deep enough to penetrate through the whole MQW active area, then filled with a blend of quantum dots (QDs) deposited through a spin coating process.



(a) Schematic representation, (b) cross-sectional, and (c) top SEM images of a photonic quasi-crystal LED hybridized with QD color converters.

In their Optica paper "Hybrid photonic crystal light-emitting diode renders 123% color conversion effective quantum yield", the researchers see this hybridization and the specific quasi-crystal geometry they chose as key factors.

When used for LED colour conversion, colloidal quantum dots (QDs) are usually dispersed into an encapsulation layer above the active LED structure, missing out the majority of the light emitted by the LED (60% to 80% of which remaining trapped within the epitaxy layers due to total internal reflection).

With this hybrid architecture, the QD emitters are placed in close proximity to the multiple quantum wells (MQWs) of the active area. This, the authors write, improves the out-coupling efficiency between MQWs and QDs, simultaneously allowing for a non-radiative resonant energy transfer between the MQWs and the QDs and near-field radiative coupling of trapped (guided) modes in the LED to the emitters.

What's more, due to its highly symmetrical far-field beam shape, the 12-fold symmetric photonic quasi-crystal exhibits long-range order and short-range disorder and possesses semi-random properties, further increasing light extraction compared to traditional photonic crystals.

The researchers report effective quantum yields for the QD emitters reaching 123% for single QD species colour converters, and around 110% for a white blend of three commercially available QDs (emitting at 535, 585 and 630nm) achieving a quasi-perfect 6500 K D65 spectrum. They think these performances could be further improved by using state-of-the-art nanocrystalline emitters.

Solar cell efficiency pushed to 35%

By Nick Flaherty

Researchers in Australia have hit a new record for the efficiency of solar cells.

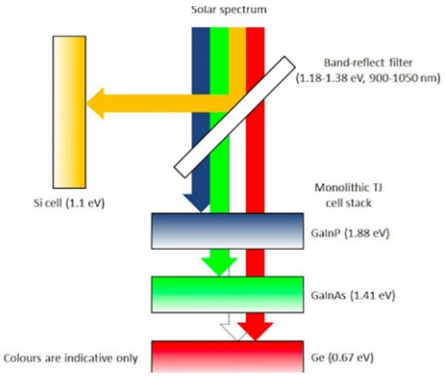
A new solar cell configuration developed by engineers at the University of New South Wales has pushed the efficiency of solar cells to 34.5%, a new world record for unfocused sunlight.

The experimental set up uses a 28cm^2 four-junction mini-module embedded in a prism to extracts the maximum energy from sunlight. It does this by splitting the incoming rays into four bands, using a hybrid four-junction receiver to absorb different frequencies in the separate layers.

The UNSW result, confirmed by the US National Renewable Energy Laboratory, is almost 44% better than the previous record – made by Alta Devices of the USA, which reached 24% efficiency, but over a larger surface area of 800cm^2.

"This encouraging result shows that there are still advances to come in photovoltaics research to make solar cells even more efficient," said Dr Mark Keevers, Senior Research Fellow of UNSW's Australian Centre for Advanced Photovoltaics. "Extracting more energy from every beam of sunlight is critical to reducing the cost of electricity generated by solar cells as it lowers the investment needed, and delivering payback faster."

A recent study by Germany's Agora Energiewende think tank set an aggressive target of 35% efficiency by 2050 for a module that uses un-concentrated sunlight, such as the standard ones on family homes.



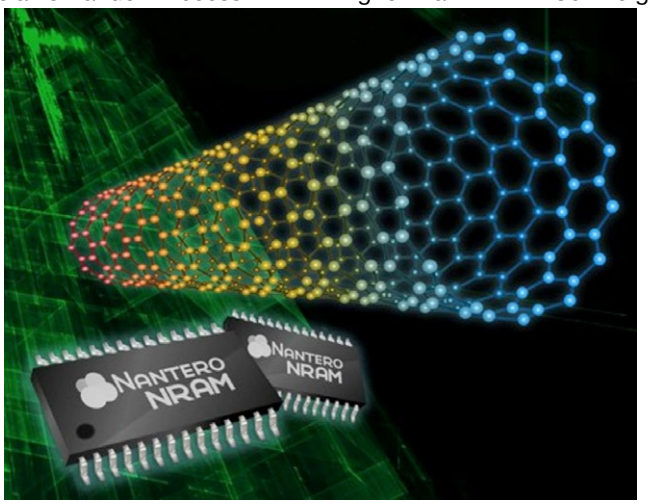
The triple-junction cell targets discrete bands of the incoming sunlight, using a combination of three layers: indium-gallium-phosphide; indium-gallium-arsenide; and germanium. As sunlight passes through each layer, energy is extracted by each junction at its most efficient wavelength, while the unused part of the light passes through to the next layer, and so on. Some of the infrared band of incoming sunlight, unused by the triple-junction cell, is filtered out and bounced onto the silicon cell, thereby extracting just about all of the energy from each beam of sunlight hitting the mini-module.

Scaling the cell up to a larger 800cm^2 is well within reach, says Keevers. "There'll be some marginal loss from interconnection in the scale-up, but we are so far ahead that it's entirely feasible," he said. The theoretical limit for such a four-junction device is thought to be 53%, which puts the UNSW result two-thirds of the way there.

Nanotube-based NRAMs taking over the world soon, says Nantero

By Julien Happich

Founded in 2001, shortly after CTO and Co-Founder Dr. Tom Rueckes had published his seminal Science paper "Carbon Nanotube-Based Nonvolatile Random Access Memory for Molecular Computing", Nantero is now confident it will take a big chunk out of the $85+ Billion memory market.



Back in July 2000, the paper was laying the foundations for a bistable non-volatile RAM cell to be designed with a suspended Single Wall Carbon Nano Tubes (SWCNTs) crossbar array, switchable into well-defined Off and On states. The device being designed in such a way that each state represent a potential energy minimum (a balance between elastic energy in the Off state and the van der Waals energy in the On state), switched by charging the nanotubes to produce attractive or repulsive electrostatic forces.

In his paper describing the 1 transistor SWNT NRAM cell, Rueckes had established possible switching speeds up to 100GHz for a 20nm device, extrapolating this to 200GHz operation for a cell designed at the 5nm node (owing to the smaller effective mass of the moving CNTs). Other claims are that the NRAM operates at orders of magnitude more cycles than flash (over 10^{11} program endurance) and retains memory for over 10 years at 300°C (could be over a thousand years at 85°C).

Since then, the startup has secured an extensive patent portfolio (175+ US patents issued and over 200 patent applications pending, including internationally) and boasts a dozen high profile customers lining up to license its IP.

The company expects both foundries and OEMs to license the IP, for some to embed the CMOS-compatible NRAM within chip designs, and for others to produce DDR4-compatible multi-GByte arrays as pure memory chips.

"We want to be the ARM of the memory business", said Greg Schmergel, Nantero's CEO and Co-founder in an interview with *EETimes Europe*.

For practical manufacturing purposes and because today no lithographic equipment would reach the 2nm level of precision equivalent to a CNT's diameter, the actual switches do not rely on single CNTs but rather on a random mesh of hundreds of CNTs with many different intersection points, explained the CEO.

"Lithography is our main limiting factor, we deposit the carbon nanotubes through a spin coating process before patterning the switches, so our technology can scale pretty much as far as lithography can go" he said.

"For now, we see most design efforts around the 2x nm node, typically 28nm, and our customers achieve densities higher than DRAM" Schmergel said, hinting that the first product tape-outs were due for the end of the year.

"We wanted to design 15nm prototypes, but we couldn't access any lithographic equipment with resolutions below 15nm" he added, reminding us that the initial claims of the paper were that the NRAM cells could be built with as few as two nanotubes.

On the upside of having random bundles of carbon nanotubes acting as bulk switches is the fact that the same NRAM device could be run either as a single-level memory (one bit per switch) or on multi-levels (several bits per switch) providing the appropriate encoding schemes are used.

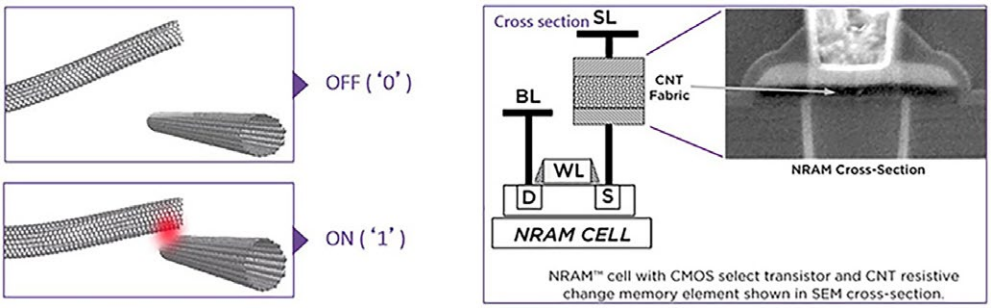
"It would essentially be the same structure, you would not need to re-engineer the device to move to a multi-level memory device", confirmed Schmergel, adding that for the next few years, the company would focus on single-level memory devices.

So how cost-competitive will these devices be?

"For embedded memory, we have a cost advantage because we use less power than embedded flash, there is also less overhead circuitry and our process only requires one or two mask layers versus many masks for flash" Schmergel says.

The CEO expects NRAM to compete with standalone DRAM in the near term, while it could take longer to beat flash on cost alone. But as customers move to smaller nodes and ramp up their production, then CNT-based memory could end up consolidating the memory marketing, eventually replacing multiple memory chips into one fast nonvolatile memory chip.

The bi-stable CNT switches could also be used as configurable logic tables, Nantero also has IP for sensors, interconnects and loss-less transistors, but is not actively commercializing it for now.



NRAM switch working principle (left) and physical implementation (right).

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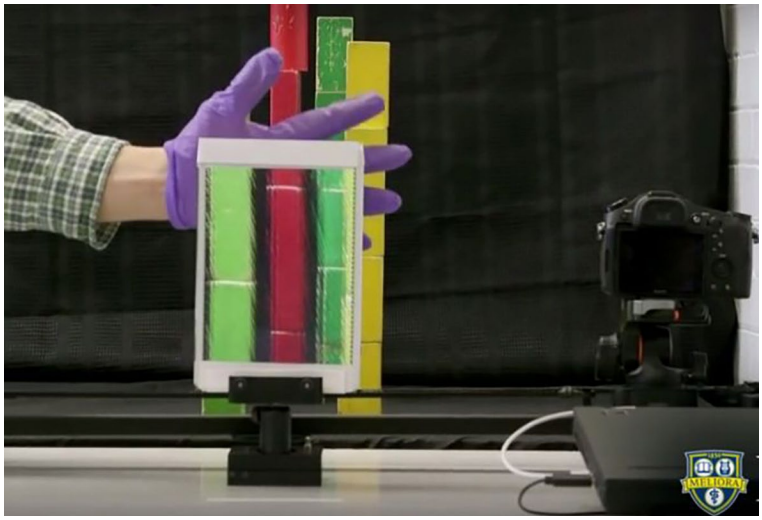
Toward a digitally reconfigurable optical cloak

By Julien Happich

In their recent Optica paper "digital integral cloak", researchers from the University of Rochester combine a scanning camera on one side and an LCD display overlaid with an array of micro-lenses on the other side of the object to be concealed, together with ray-tracing algorithms running in between.



The proof-of-concept demonstration tricks the eyes into seeing what's behind the cloaked object as if the light rays were directly passing through the "invisible" object.

The cloak is reconfigurable in the sense that if the background changes, the output can be updated through another scan of the background area by the camera, with ray-tracing algorithms put into play to compute the right display rendering on the LCD so each micro-lens redi-rects the right colours in the right directions (the maths have to take into account the depth of the concealed zone).

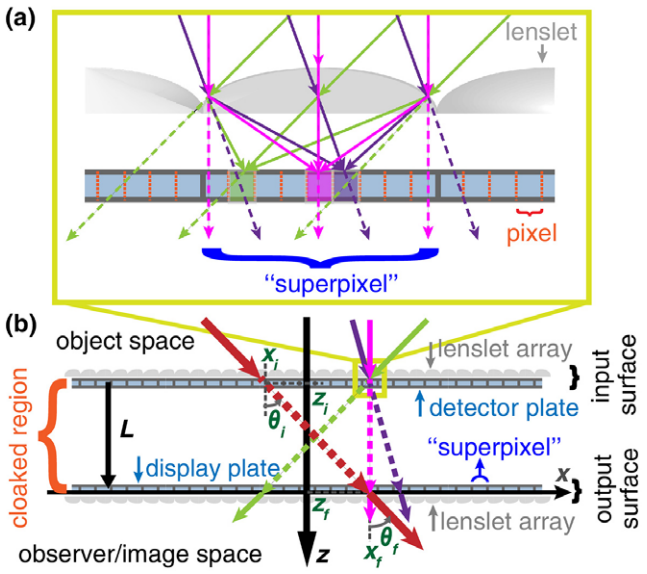
The thin, parallel semi-cylindrical micro-lenses then recreate multiple images of the background, hence perfecting the illusion regardless of the viewer's position (a considerable improvement over a flat 2D rendering which would equate to intercalating a poster of the background).

Because the proof-of-concept experiment only used a camera mounted onto a rail for scanning the background, it took PhD student Joseph Choi and his advisor Professor of Physics John Howell several minutes to scan, pro-cess and update the image on the screen for every change in background.

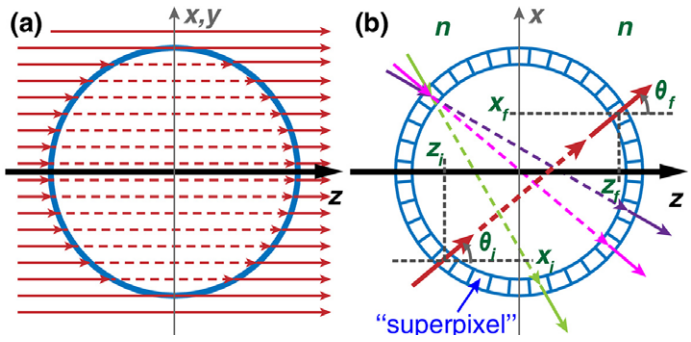
But in the future, Choi envisages that one side of the object to be concealed could be covered with a lenticular array of optical sensors, and a conformable lenticular display onto its other side showing the right pixels in all directions so as to show the background as if the object weren't there. A fixed setup would only work as long as the object's shape wouldn't change, the geometry and spatial location of the optical sensors being taken into con-sideration in the mathematical model to compute which pixels to feed on the output display.

Pushing the concept further, the author concludes that the surface of the cloak could be discretized with so-called superpixels that could both detect and emit multiple discrete ray positions and angles. Combined with enough computational power, such a digital cloak could function in real-time for just any object shape, allowing for wearable and deformable cloaks. Increasing display resolutions and ever shrinking flexible sensor technologies could turn such an implementation into reality, Choi thinks.

The Rochester Digital Cloak is patent pending and the university is open for business to further its research into a commercial product.



Cross section of a digital integral cloak showing two parallel 2D surfaces, with a few sample rays. The input "surface" (lens array and plate) captures input light rays. The output surface displays rays as if they passed through ambient space only (dashed lines). Superpixels, placed at the focusing plane of a lenslet, collect rays with the same position as the lens. These rays are then spatially separated into pixels, such that one ray angle (or "view") maps to one pixel. Display (output) is the reverse of the detection scheme.



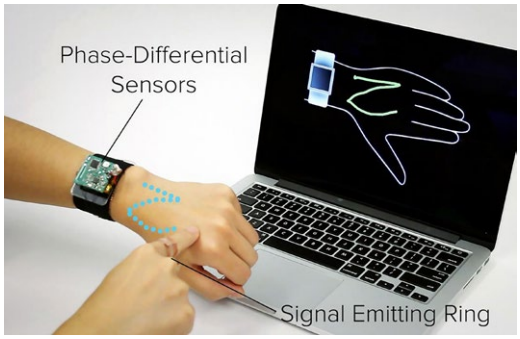
Concept of an ideal spherically symmetric cloak with example rays (solid arrows) entering and exiting the cloak. Dashed arrows show how the rays appear to have traveled inside the cloak (where objects are invisible). Such a cloak would be omnidirectional.

SkinTrack technology turns arm into touchpad

By Jean-Pierre Joosting

Wearable technology developed at Carnegie Mellon University suggests turning the entire lower arm into a touchpad could be a sloultion to the tiny interface presented by smartwatches.

Called SkinTrack and developed by the Human-Computer Interaction Institute's Future Interfaces Group, the system allows for continuous touch tracking on the hands and arms. It also can detect touches at discrete locations on the skin, enabling functionality similar to buttons or slider controls. Previous "skin to screen" approaches have employed flexible overlays, interactive textiles and projector/camera combinations that can be cumbersome. SkinTrack, by contrast, requires only that the user wear a special ring, which propagates a low-energy, high-frequency signal through the skin when the finger touches or nears the skin surface.



Carnegie Mellon University's SkinTrack enables users to turn their skin into a touchpad for controlling smartwatches.

"The great thing about SkinTrack is that it's not obtrusive; watches and rings are items that people already wear every day," said Yang Zhang, a first-year Ph.D. student in HCII."A major problem with smartwatches and other digital jewelry is that their screens are so tiny," said Gierad Laput, a Ph.D. student in HCII and part of the research team. "Not only is the interaction area small, but your finger actually blocks much of the screen when you're using it. Input tends to be pretty basic, confined to a few buttons or some directional swipes."

"SkinTrack makes it possible to move interactions from the screen onto the arm, providing much larger interface," said Chris Harrison, assistant professor in the HCII and adviser to the research. The user wears a ring that produces a high-frequency electrical signal. When the finger gets near to the skin or touches the skin, that signal propagates through the skin.

By using electrodes integrated into the watch's strap, it's possible to pinpoint the source of those electromagnetic waves because the phase of the waves will vary. Electrodes corresponding to the 12 o'clock and 6 o'clock positions on the watch, for instance, can detect phase differences that can determine the position of the finger along the width of the arm; electrodes at the 3 o'clock and 9 o'clock positions can determine the finger's position along the length of the arm.

The researchers found that they could determine when the finger was touching the skin with 99 percent accuracy and they could resolve the location of the touches with a mean error of 7.6 millimeters. That compares well with other on-body finger-tracking systems and approaches touchscreen-like accuracy.

The researchers showed that SkinTrack could be used as a game controller, to scroll through lists on the smartwatch, to zoom in and out of onscreen maps, and to draw. A number pad application enabled users to use the back of the hand as a dial pad for the onscreen number pad; hovering a finger over the hand acts as a cursor, highlighting numbers on the screen to aid in targeting touch points. The system has some limitations. Keeping the ring powered up is a challenge. Signals also tend to change as the device is worn for long periods, thanks to factors such as sweat and hydration and the fact the body is in constant motion.

The technology is safe. No evidence suggests that the radio frequency signals used by SkinTrack have any health effects. The body is commonly excited by daily appliances – everything from the tiny amounts of current drawn from the finger by touchscreens to the electromagnetic noise emanating from fluorescent lights – with no ill effects.

Android N joins auto OS battle

By Junko Yoshida

This auto-centric variant of Android N OS—natively running in a car—would allow carmakers to develop infotainment systems that can access heating and air conditioning, AM/FM radio, connectivity and other core functions besides the usual media, navigation and messaging apps.

Google showed off Android N on a reference In-Vehicle Infotainment (IVI) concept system inside a Maserati Ghibli. The system featured a vertical 15-inch screen—much like the one you find in Tesla today—and high-definition digital instrument cluster powered by Qualcomm's Snapdragon 820 chip.

What changed?

Up until now, Google has not offered "auto-specific middleware to control infotainment systems," Egil Juliussen, senior director & principal analyst IHS Automotive, told *EE Times*. The lack of a middleware standard has sent car OEMs and Tier Ones scrambling for proprietary middleware or some version of Linux OS for in-vehicle infotainment systems.

Undoubtedly, Android N will give Google a much deeper inroad into the automotive market. It allows Google to offer automakers a range of apps and services from which to choose.

More important, when Google does this middleware, "it becomes a standard that will be updated by Google," said Juliussen. "It saves the OEMs from doing so."

Ultimately, Google's move will lead to a shakeup of embedded operating systems – especially the growing number of different versions of Linux OS currently proliferating on the automotive market.

Android N OS running on screens (of head unit and instrument cluster) inside Maserati Ghibli (Source: Google)

IHS predicts Google's move will "consolidate the many Linux OS versions to two—Android N OS and GENIVI-compliant OS (and potentially a Chinese-centric Linux variant, such as YunOS, which is essentially a forked version of Android)."

GENIVI is a Linux-based operating system, middleware and open-source development platform for the automotive in-vehicle infotainment (IVI) industry, grown out of GENIVI Alliance—founded in 2009 by BMW Group, Delphi, GM, Intel, Magneti-Marelli, PSA Peugeot Citroen, Visteon, and Wind River Systems.

Juliussen foresees a future OS battle in the IVI market primarily fought among QNX, GENIVI Linux and Android Linux. Meanwhile, Android N OS will "hasten the phase-out of the auto version of Microsoft Windows Embedded and other proprietary OS products," he added.

But how will QNX—owned by Blackberry—hold up against Android N?

Juliussen observed that QNX is well prepared for an infotainment Android N OS because BlackBerry has developed a software emulation of Android APIs. "This means that QNX can co-exist with Android Auto and Android N OS better than its competitors in most cases," he noted.

However, IHS expects QNX's dominant share in infotainment OS to "decline somewhat by the introduction of Android N." The research firm predicts that Android N could reach 35 percent globally sometime after 2020.

How close to commercialization?

Today, Android N isn't the final name, and there is no commercial name for the auto-centric variant of Android N, either.

But this could quickly change.

IHS pointed out that General Motors and Harman earlier announced a partnership to build Android-based infotainment systems for GM vehicles. "This $900 million contract will bore a new next-generation infotainment system powered by Android by the end of 2016—it's possible that those vehicles will be powered by this Android embedded system," said IHS analysts in their research note.

The Google-designed interface will be offered free to automakers. Most likely, OEMs will develop their own HMI – or skin – over the Android N OS.

Judging from how Google has changed the smartphone market with Android OS, it could do the same to the IVI market – simply by following the same playbook.

No one has measured OEMs' enthusiasm or resistance. But Google is counting on its app store and core services to entice carmakers to go with Android N.

Qualcomm gets a foot in the door

Qualcomm has played a key role working with Google to embed the power of the Android OS into the car.

Just as Qualcomm's Snapdragon processors have dominated the Android smartphone market, Qualcomm sees a big opportunity for its auto-grade Snapdragon processors to star in connected cars and infotainment systems.

The concept car functions demonstrated at Google I/O used Qualcomm's Snapdragon 820A integrated with CPU, GPU, X12 LTE modem (capable of Cat 12 speeds) and video processing capabilities.

Qualcomm believes the creation of infotainment systems

using Android as a common platform will make it easier for OEMs and Tier Ones "to add connected services and applications, and accelerate innovation in the car."

Android Auto

Google developed Android Auto as a smartphone projection standard. It allows mobile devices running the Android OS – connected over USB or Bluetooth – to be projected on the dashboard's head unit and operated in cars.

Now that Android N could do so much more, what will happen to Android Auto?

At Google I/O this week, Google announced that Android Auto will work as a standalone app in the car. In short, Google will untether Android Auto from the dashboard, so that an updated Android Auto app can work independently of infotainment systems.

IHS believes that this is a right strategy. It means drivers with older cars or no infotainment systems can simply "mount their phone and still get the benefits of Android Auto," the research firm said.

Such moves "will dramatically increase the potential market of Android Auto app users, and that with the increased potential customer base, many more apps will be announced for Android Auto," according to IHS. "We expect many of those apps will seamlessly work with Android's IVI OS system, too."

IoT piggybacks on Lego: simple physics

By Julien Happich

Doing quantum physics research at the Tel Aviv University, Boaz Almog is probably best known for his papers about quantum levitation when together with Barak Deutscher from the superconductivity group at Tel-Aviv University, he demonstrated over fifteen years ago how a superconductor disk can be trapped in a surrounding magnetic field.

Since then, the quantum physicist has been busy educating the masses about superconductivity, both through public demonstrations and more recently by commercializing demonstration kits via his company, Quantum Experience - www.quantum-levitation.com – founded in 2013.

Yet, the CEO started up another company in June last year, Brixo Smart Toys ltd, with the scope to commercialize Lego-compatible electronic bricks. Running a crowdfunding campaign on KickStarter and only with a few hours left, the Israeli startup has raised well over ten times its initial $50,000 goal, offering what it describes as Lego on steroids.

The chrome-plated bricks can conduct electricity, integrate active parts such as LED lights, motor blocks, and even sound, light and proximity sensors. The conductive bricks feature flexible side-arms that ensure electrical connection between two adjacent blocks, and the whole assemblies are powered by a Bluetooth-controlled 9V battery block. The built-in Bluetooth controller lets users change the current's direction and voltage levels via a mobile application.

That means the Brixo bricks can not only be triggered by sound, light and touch, but also controlled by any Bluetooth connected device, taking the good old Lego bricks further into the IoT world (the Danish company already has its entries in the cloud via its Mindstorms Lego series and the augmented-reality capable Nexo Knights toys).

The company is promising open 3D building instructions, an online library of models and hacks to its followers, encouraging a community of Brixo enthusiasts to share their models.

Stretchable polymer optics embed carbon nanotubes for better focus

By Julien Happich

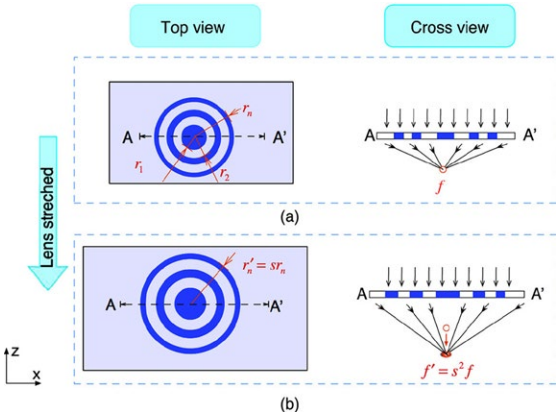
Researchers from the Department of Microelectronics at the Delft University of Technology have flattened out the binary Fresnel lens concept to a thin stretchable polymer membrane with radial patterns of vertically grown carbon nanotubes (CNT). The integration of CNTs, grown perpendicular to the optical plane, ensures a very high optical absorption (a transmittance of only 0.06% in the visible light spectrum versus the 93.9% transmittance of the PDMS membrane), hence a very good contrast to spatially modulate the intensity distribution of the light passing through the diffraction patterns of the binary Fresnel lens.

The carbon nanotubes are grown in concentric rings only 10µm high, before being percolated with polydimethylsiloxane and being peeled off with the stretchable membrane. This makes such diffractive optics only a few tens of micron thick.

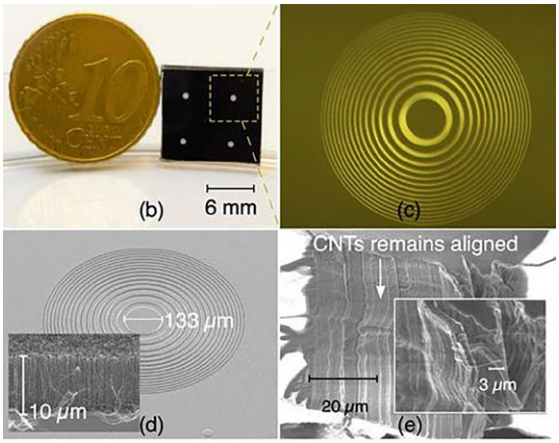
In their paper "Stretchable Binary Fresnel Lens for Focus Tuning", the researchers report their results using lenses that are 6×6mm square with a focal length tuneable from 7mm to about 9mm by radially stretching the lens a few percent of elongation. Although they experienced some distortion due to the clamping system they used to stretch the lens, an integrated circular actuator could certainly solve the issue, providing a uniform radial deformation.

Lead author Xueming Li is keen to highlight that although the paper only mentions a 7mm focal length, the researchers worked on other focal lengths.

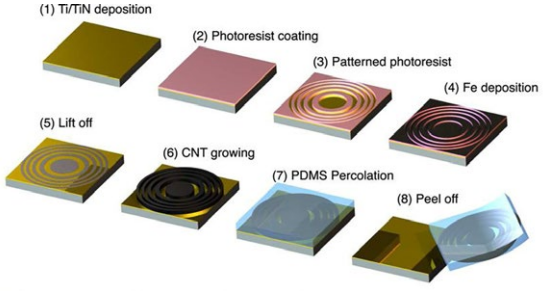
"Using the same concept and fabrication process, we fabricated lenses with focal lengths ranging from 100µm to 20mm, so to match application specific demands.



When stretching the flexible substrate radially by s from (a) to (b), the radius of the n^{th} zone increases from r_n to r'_n and the focal length changes from f to f' by a factor of s^2.



(b) A fabricated device containing 2×2 lens units, with each unit 6×6mm² in size. (b) An optical microscopy image of a single lens and (c) a SEM image of a single lens unit, with 7mm in focal length and an innermost zone diameter of 133µm, before PDMS infiltration. (e) shows the CNT inside the PDMS well aligned after the PDMS percolation forming the CNT/PDMS composite.



For instance, a focal length ranging from 5µm to 8.5mm can be used in microscopy to investigate fluorescence signals. Lens arrays with focal length ranging from 2mm to 20mm can be used for compound eye applications and point of care devices" Li wrote *EETimes Europe*.

"Due to the controllable variable focal length, this configuration can also be applied to multi-focus contact lens applications" he added.

Referring to competing research performed with less adaptive rigid materials such as black silicon for the opaque material instead of CNTs, Li notes: "The advantages of using CNTs are first, the porous character of the layer, which allows the PDMS to better penetrate in the CNTs. This is important for radial control when stretching the lens. Secondly, the fabrication of CNTs is more controllable than black silicon, which makes it a more reliable process for large scale device manufacturing. The fabrication of our lens (array), of which the key process is the growth of patterned CNTs, is fast and reliable. Moreover, as a commercially available CVD system is used, and a wafer scale process is developed, it is possible to scale up the area for large volume manufacturing of these devices".

Li sees such flat optics find their way into miniaturized photonic chips, integrated optics, optical interconnects, beam focusing or maskless lithography systems, but also for deflecting and collimating tasks in optical sensor systems or for optical data transfers.

"The low cost and scalable manufacturability of our device provides solutions for disposable microscopes, which are valuable for health diagnostics in developing countries" he explained.

On the left, the main fabrication steps: (1) Ti/TiN (10nm/50nm) is sputtered on a silicon wafer to prevent diffusion of the catalyst into the substrate; (2) 1.4µm photoresist is coated and (3) patterned on the wafer; (4) Iron (5nm) is evaporated as catalyst, followed by (5) a lift-off process to define the CNT growth regions; (6) Vertically aligned CNT bundles (10µm in height) are grown by CVD, (7) PDMS is poured on the horizontal silicon wafer substrate with the defined CNT patterns. After degassing, the device is released by peeling off the PDMS layer together with the encapsulated CNT from the silicon substrate (8).

IR-based ToF for lightweight 3D mapping

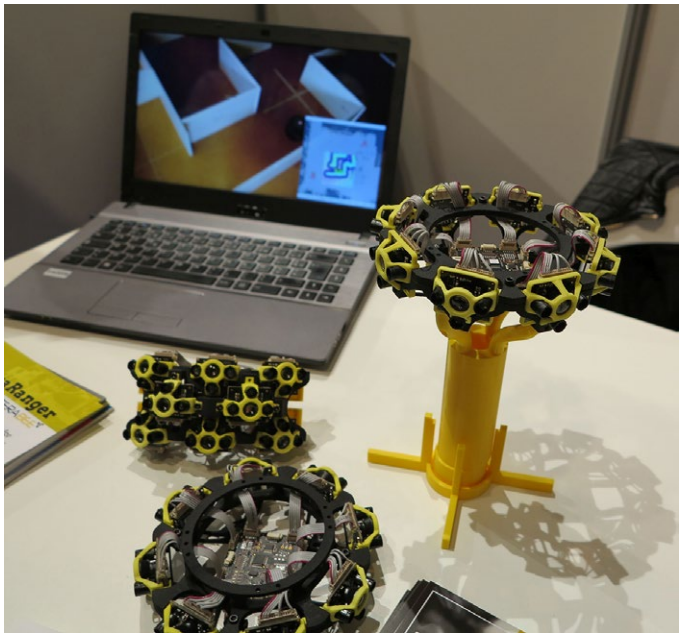
By Julien Happich

Working deeply with CERN (European Centre for Nuclear Research) in 2012, French startup Terabee has taken IR-based time-of-flight (ToF) to centimetre-level, boasting update frequencies up to 1kHz for fast moving robots and drones.

The company's lead product, TeraRanger One, is a 35x29x18mm standalone device weighing only 8 grams.

Because the ToF unit only packs three eye-safe IR LEDs and a centrally-designed IR sensor to stream calibrated distances in mm, the static design is more reliable than bulkier rotating laser lidars typically used in Simultaneous Localisation and Mapping (SLAM) robotic applications.

Several static sensors are already designed into arrays, linear or circular, for a wider field of view (3° per unit), and a single unit was even mounted onto a motor spindle to emulate a lidar.

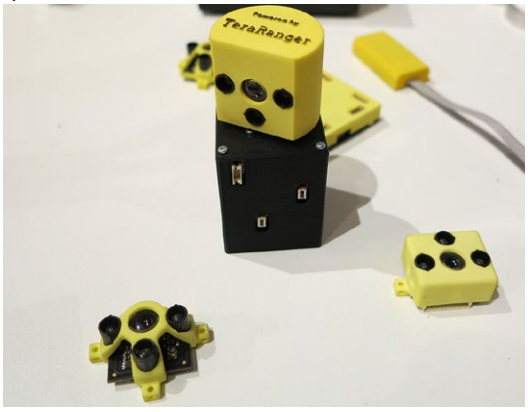


The TeraRanger Tower is demoed in a video. Terabee also builds custom arrays.

"The original product idea came up from a joint project at CERN, to automate the visual inspection of the Large Hadron Collider's 27km+ tunnel", Commercial Manager Greg Watts told *EETimes Europe*.

The researchers evaluated a number of collision-avoidance technologies to mount on top of a small drone but soon realized that none of what was available on the market was fast and accurate enough to meet their needs, flying through the tunnel and over their complex installations.

With a detection range of 20cm to 14 meters (6m outdoors on the Type A first generation sensor, but now 14m with Type B) and its fast acquisition speed, the TeraRanger One found many other applications since then and is currently being tried by hundreds of customers, according to the company.



The TeraBee One in spider (left) and box (right) versions, and a rotating lidar.

Terabee's CEO Max Ruffo told us the company had already gone through several rounds of financing, raising a few million euros for its industrialization phase. "Today, we are not desperate for more cash, we are seeking strong partnerships to pursue the integration of our products and to gain access to a wider market", Ruffo said, adding that with only about 15 shareholders (some of them working at Terabee), the privately owned company was under no external pressure.

"We have development projects with several high-profile customers and we have secured a good supply chain so we can readily ship in the thousands and hundreds of thousands of units" the CEO said, shy of disclosing any real figures.

During the Innorobo event in Paris, Terabee exhibited the TeraRanger Hub, a plug-and-play microprocessor module able to manage up to eight sensors, an entry-level rotating lidar scanner for short-range indoor applications (with one sensor mounted onto a motor spindle), and the TeraRanger Tower simultaneously streaming the distance data of eight sensors arranged in a circular fashion (with 45° between each sensor axis). A demo video was also running, showing a robot navigating autonomously through a reconfigurable maze.

The company is happy to develop custom arrangements to meet specific needs, but it is not stopping there. Showing the tiny TeraRanger One in his hand, Ruffo unveiled his vision for the future.

"We are looking at shrinking our technology further and in fact, we are now developing multi-pixel arrays the size of this box. Eventually, we want to achieve active 3D vision with point clouds and depth as a simple output ", he concluded.

Microsoft shines light on HoloLens

By Rick Merritt

Microsoft gave a look inside its HoloLens and the Holographic Processing Unit that drives it at the Imec Technology Forum. The HPU is among an emerging class of specialty accelerators.

In late March, Microsoft started shipping a developer's version of HoloLens, its novel augmented reality goggles. The release generated a flood of teardowns but until now they lacked commentary from the headset's designer.

"We have showed HoloLens for last 18 months, focusing usually on the experience and the software -- this is the first time we will talk about the hardware," said Ilan Spillinger, corporate vice president of HoloLens and silicon at Microsoft.

The HPU at the core of the headset is essentially a data fusion sensor. It takes inputs from an array of sensors on the HoloLens include four environmental sensors, a miniaturized Kinect depth camera and an inertia measurement unit. It accelerates algorithms that track the user's environment, movements and gestures and displays holographic images.

The 28nm HPU is essentially a highly customized DSP array running at less than 10W max. It includes an unknown number of Tensilica DSP cores optimized to run hundreds of HoloLens-specific instructions.

Each core is customized for a particular function and subset of instructions. In what sounds like a non Von Neumann architecture, each typically has its own unique organization of related memory units. It accelerates "new style algorithms that need special local memories and a unique memory architecture, not a typical level 1-2-3 cache," he said.

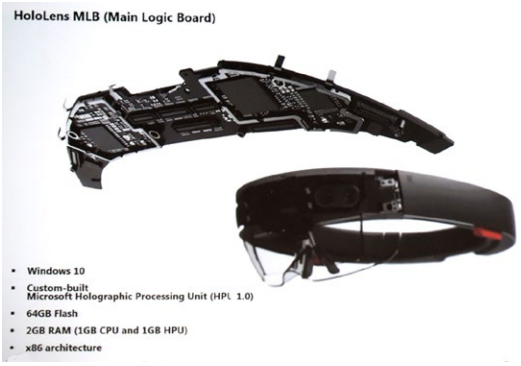
The headset is powered by a 14nm Intel Cherry Trail SoC with embedded graphics running Windows 10. The two-sided motherboard also contains 64 Gbytes flash storage and 2 Gbytes external memory split evenly between the HPU and Cherry Trail SoCs.

Spillinger would not comment on the road map for the HPU except to say he "sees opportunity for running algorithms we didn't think about."

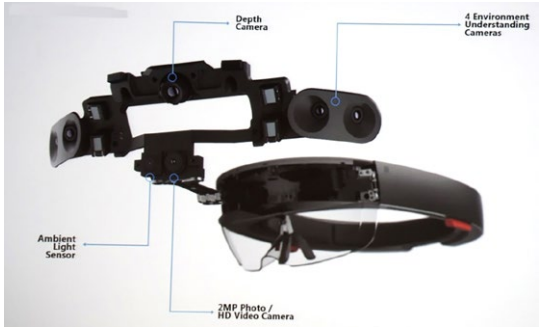
The HPU fits roughly in the category of a new accelerator Google announced last week for its data centers as well as one in the works at a startup.

Spillinger called on semiconductor engineers to pave a road to higher performance, lower power chips to help him build lighter, cheaper headsets packing more sensors and features.

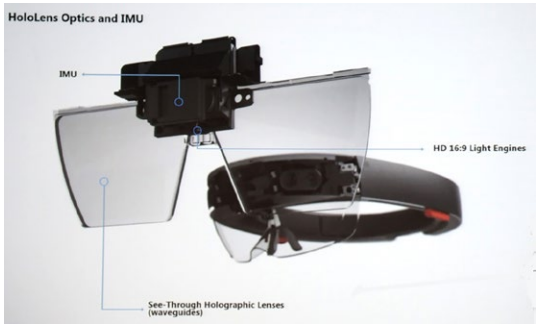
The HoloLens chief started his career at Intel working on Centrino, its first dedicated notebook processors.



The HoloLens HPU rides a sleek motherboard tailored to fit the headset. (Images: EE Times)



The HoloLens sensor bar packs four environmental cameras for tracking head movements and gestures used to control the display.



The HoloLens optics subassembly.

Later, he moved to IBM designing Infiniband and Power chips and later helping Microsoft and Nintendo develop ASICs for the Xbox 360 and Wii consoles.

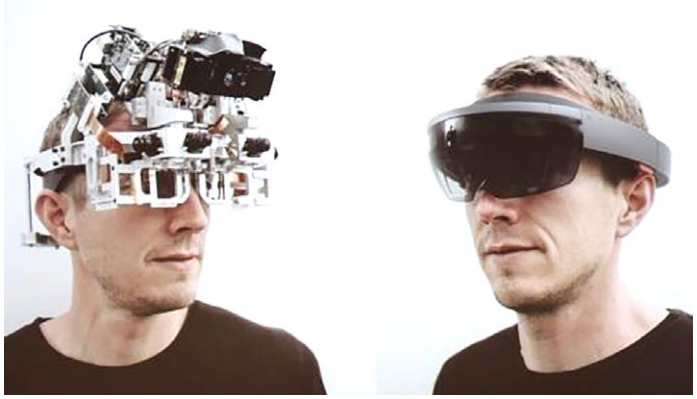
In late 2007, Spillinger joined Microsoft and started work on the Kinect. The project later merged with efforts by other engineers to develop an augmented reality headset and the HoloLens project was born.

The HoloLens sensor bar packs four environmental cameras for tracking head movements and gestures used to control the display. A depth sensor is a Kinect scaled to a fraction of its size and power consumption. It supports a short range mode for tracking gestures within a meter and a long range mode for mapping the room. A 2MPixel high def video camera projects images the user sees.

The optics subassembly includes an inertial measurement unit meeting tailored specifications. The optics use gratings developed and manufactured by Microsoft. They support a wide inter-pupil distance and adjust for users wearing contact lenses or glasses.

An LCoS display supports 2.3 million points of light and an accuracy that lets users project and read even fine text on a Web browser.

An early prototype used a full-sized Kinect depth sensor and various subassemblies eventually redesigned into a sleeker consumer form factor that packs a hefty bill of materials.

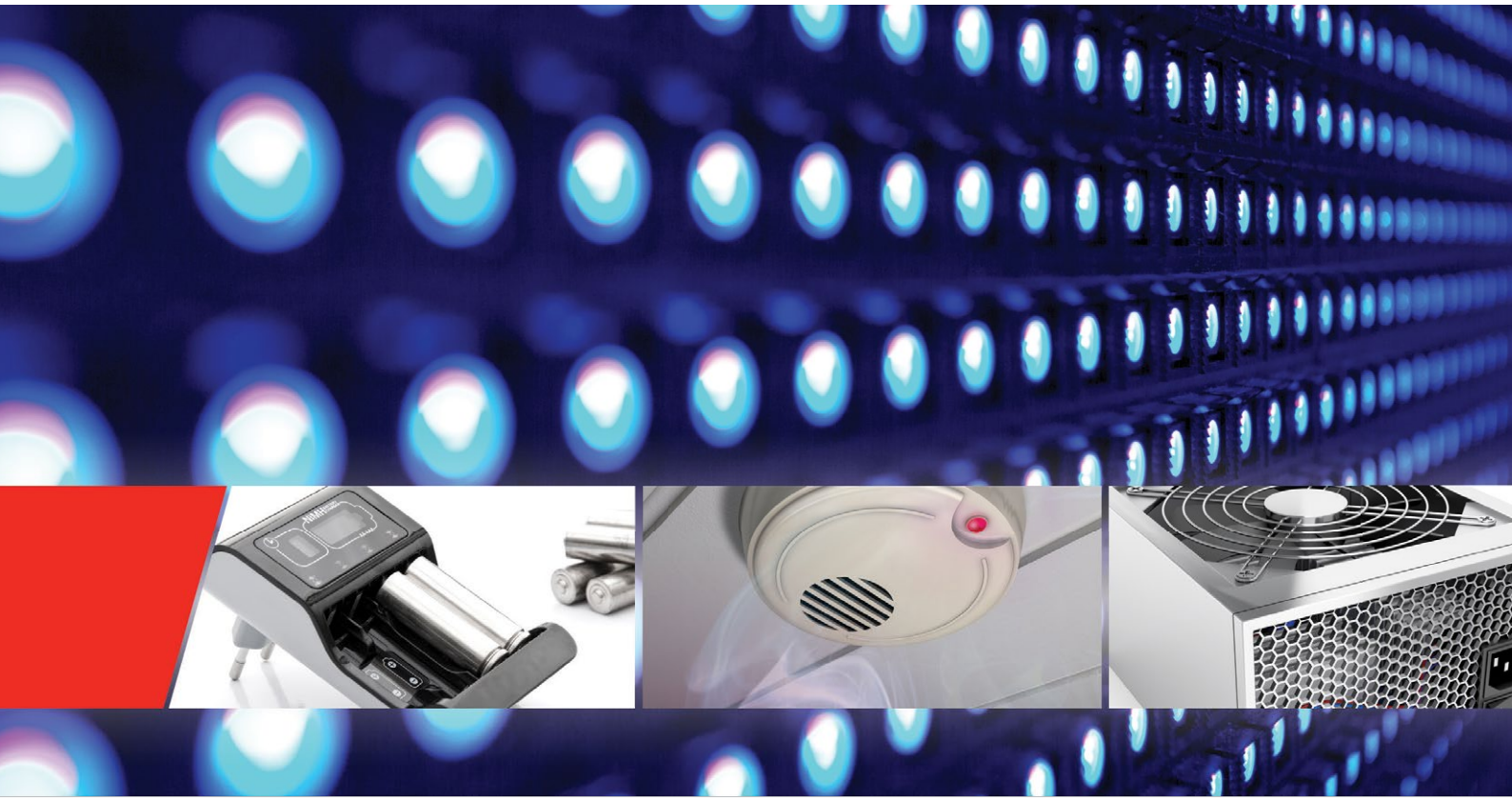


An early prototype (left) and today's developer version (right).

Analog and Interface Products

MICROCHIP

Stand-Alone Analog and Interface Solutions



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Microchip's Analog Solutions

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- Operational amplifiers with lowest current consumption over GBWP
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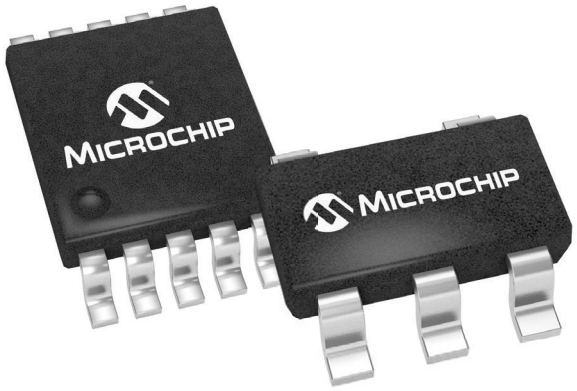


Proprietary Enabling Technology

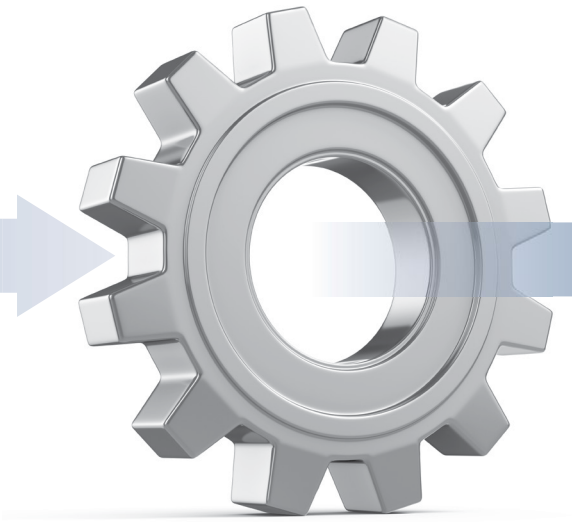
Low-Power CMOS Process
Lower power than competing processes

Understanding Customer Needs
Only necessary features are included, unnecessary power-consuming features are excluded

Simplified Designs
Proprietary designs reduce circuit complexity for more performance and less power

Expertise on Multiple Process Nodes/Advanced Lithographies
Combination of internal and external foundries utilizes the latest technologies

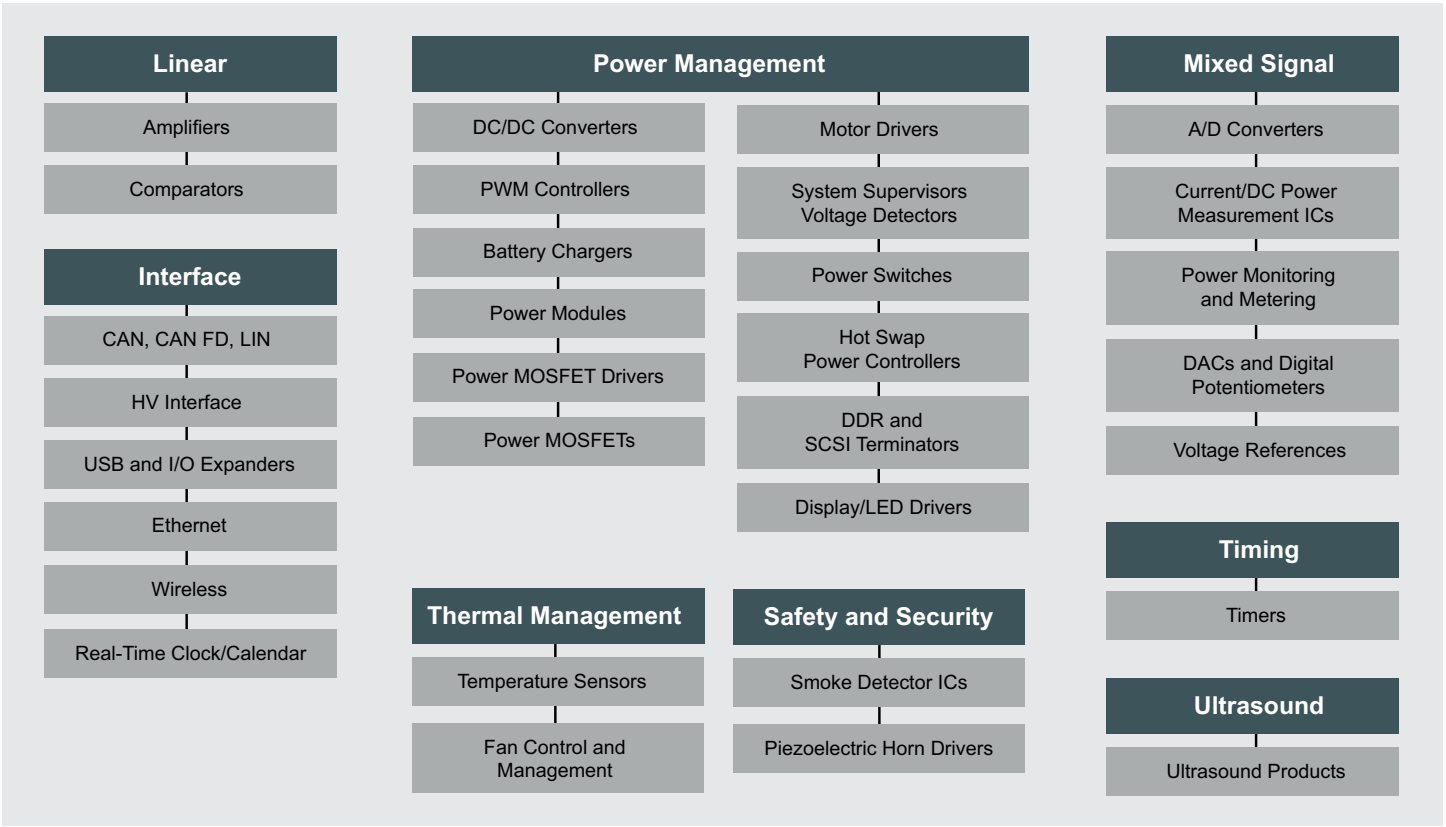
High-Voltage Technology
Offline and automotive capabilities



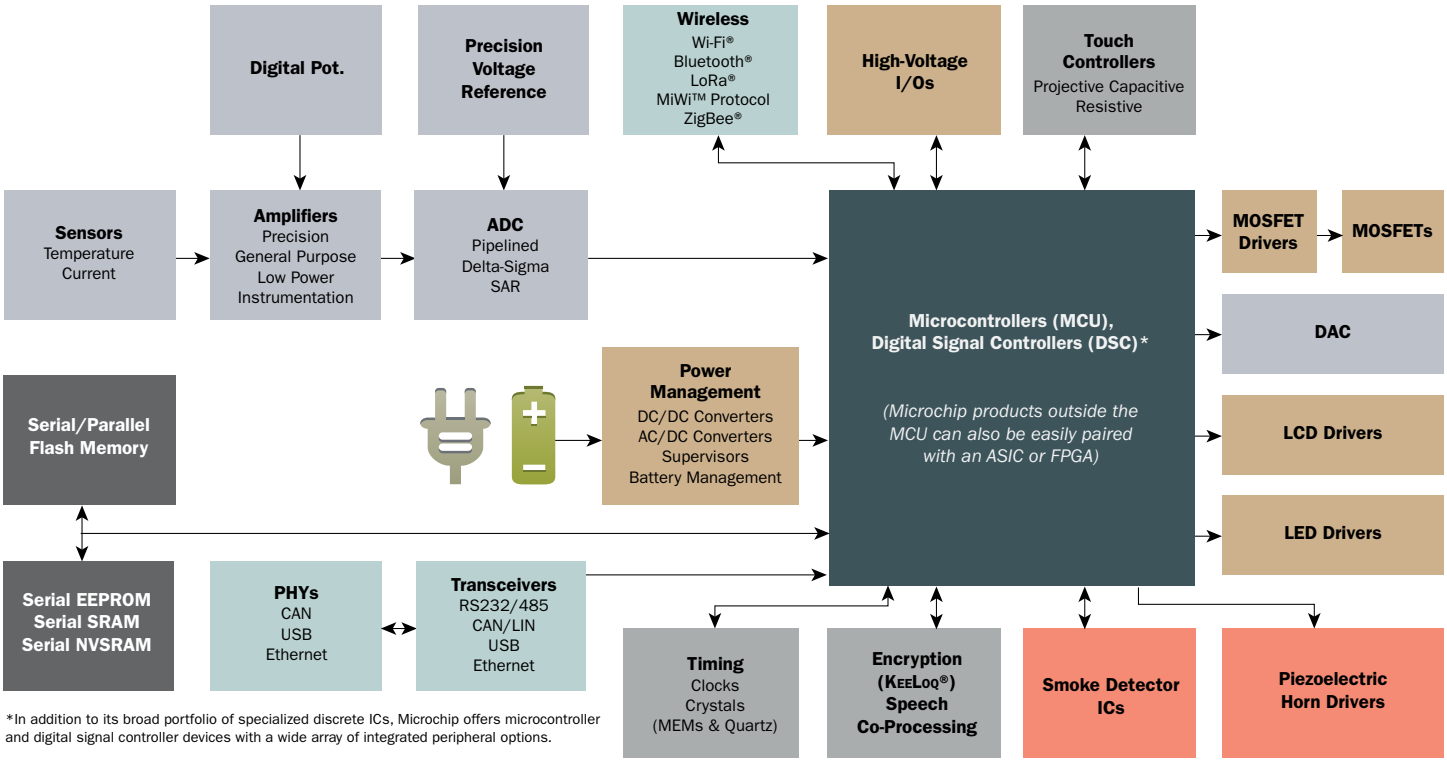
A Complete Analog Solution

Microchip's Analog Solutions

Microchip's Stand-Alone Analog and Interface Portfolio



Microchip System Support



*In addition to its broad portfolio of specialized discrete ICs, Microchip offers microcontroller and digital signal controller devices with a wide array of integrated peripheral options.

Enhanced EMI Rejection, Precision "Zero-Drift" and Low Power

Solutions for Enhanced EMI Rejection

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Microchip's family of precision "Zero-Drift" amplifiers provides superior DC performance, including ultra-low initial input offset voltage, very-low offset drift over time and temperature, superior power supply and common mode rejection and eliminates 1/f noise. This precision performance is available in select amplifier families.

- Low initial offset provides high performance for precision applications
- Very-low offset voltage drift maintains high performance over temperature variations

Featured EMIRR Solutions (Including General-Purpose and Zero-Drift Amplifiers)

Product	General Purpose	Zero-Drift	INA	EMIRR	Bandwidth
MCP642X	✓			97 dB @ 1.8 GHz	90 kHz
MCP6V6X		✓		101 dB @ 1.8 GHz	1 MHz
MCP6V7X		✓		96 dB @ 1.8 GHz	2 MHz
MCP6V8X		✓		101 dB @ 1.8 GHz	5 MHz
MCP6V9X		✓		93 dB @ 1.8 GHz	10 MHz
MCP6N16			✓	106 dB @ 1.8 GHz	500 kHz

Low-Power Solutions

Low-power, general-purpose and precision op amp solutions from Microchip provide among the industry's best power consumption performance per GBWP, including low quiescent current and exceptionally low leakage current over temperature (up to 125°C). Solutions are offered in space-saving SC-70 packages and have an operating voltage down to 1.4V.

- Provide for extended battery life in portable applications
- Reduce errors in sensor conditioning circuits due to very low leakage currents

Featured Low-Power Solutions

Product	General Purpose	Zero-Drift	Iq (typ.)	GBWP
MCP6441	✓		0.450 µA	9 kHz
MCP6V11		✓	7.5 µA	80 kHz
MCP6471	✓		100 µA	2 MHz
MCP6481	✓		240 µA	4 MHz
MCP6491	✓		530 µA	7.5 MHz

Target Applications

- Portable equipment and medical instrumentation
- Sensor conditioning
- Industrial control

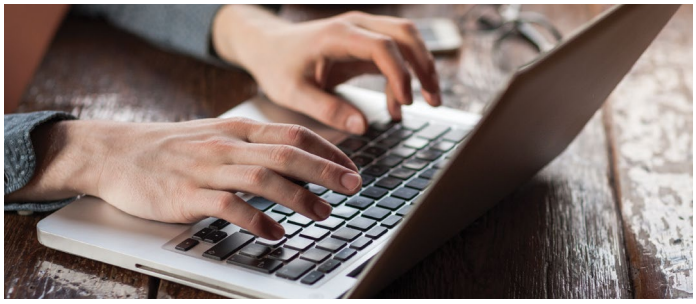
Resources

- AN1767: Solutions for Radio Frequency Electromagnetic Interference in Amplifier Circuits
- MCP6421 EMIRR Evaluation Board (ADM00443)

www.microchip.com/linear

Calibration, Trimming and Set-Point Control

Calibration, trimming and set-point control are common functions used in a wide variety of applications in the world of measurement and instrumentation. Microchip Technology offers product families to support these designs including Digital-to-Analog Converters (DACs), digital potentiometers, comparators and voltage reference devices.



Key Enabling Features

Digital-to-Analog Converters

- Fast settling time: 6 µS typical
- User-selectable voltage reference options:
  - Device V_{DD}
  - Ext. V_{REF}
  - Internal bandgap
- Non-volatile memory (EEPROM) (MCP4XFEBXX family)
- Volatile memory (MCP4XFVBXX family)
- I^2C interface (MCP47FXBXX family) and SPI interface (MCP48FXBXX family)

Digital Potentiometers

- High-voltage support (36V, ±18V)
- Resistance options: 5k, 10k, 50k, 100k
- 7-bit (128 taps) MCP4XHV31 family
- 8-bit (256 taps) MCP4XHV51 family
- Available I^2C and SPI interface

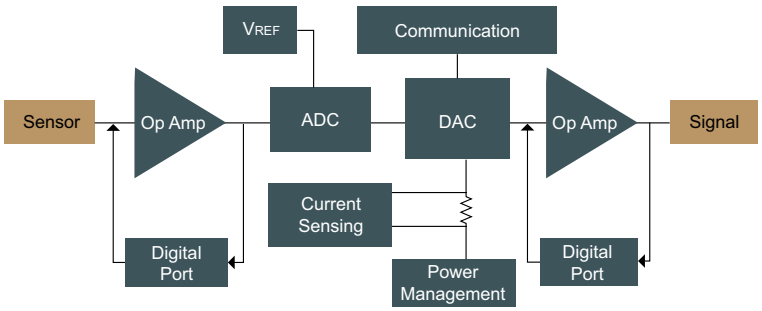
Comparators

- High-speed alternatives (47 ns prop delay)
  - MCP6561/2/4 Push-pull
  - MCP6566/7/9 Open-drain
- Low-current operation
  (Low quiescent current – 600 nA typical)
  - MCP6541/2/3/4 Push-pull
  - MCP6546/7/8/9 Open-drain
- Integrated reference (Fixed 1.21V and 2.4V options)
  - MCP65R41 Push-pull
  - MCP65R46 Open-drain
- Low-power, windowed operation
  - MIC841/2 Push-pull and open-drain
  - MIC833 Open-drain

Voltage References

- High initial accuracy of 0.08% (MCP1501)
- Popular voltage options
- Available space-saving package: 2 × 2 mm DFN (MCP1501)

Signal Chain Solutions



Target Applications

- Low-power portable instrumentation
- Test and measurement
- Precision data acquisition

www.microchip.com/dataconverters
www.microchip.com/linear

Temperature Compensation and Monitoring

Temperature Sensors

Increasing system reliability is a key concern for today's design engineer. Microchip's wide array of thermal management solutions allows you to optimize your designs based on the specific needs of your end system. Solutions with serial digital data, voltage level and logic level outputs are available. Multi-channel remote diode solutions are also available, allowing for maximum design flexibility.

Serial Digital Output Temperature Sensor – MCP9800

- DIMM Applications: Meets JEDEC Specification (MCP98244)
- Standby mode for power savings (as low as 1 µA)
- 2-wire I²C/SMBus compatible interface

Voltage Output Linear Active Thermistor – MCP9700

- Two voltage output options: 10 mV/°C and 19.5 mV/°C linear slope
- Operating current as low as 6 µA
- Small, space-saving SC-70 packages

Remote Diode Temperature Monitors – EMC114X

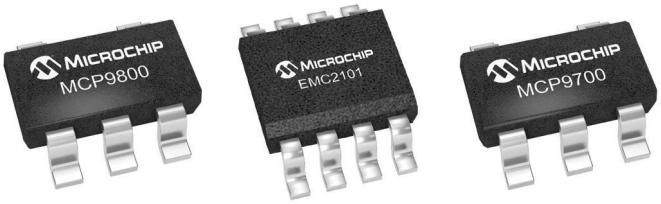
- Multi-channel temperature monitoring capability
- Resistance error correction eliminates offsets due to series resistance
- Anti-parallel diodes – require fewer traces, save board space

Logic Output Temperature Switches – MCP950X

- Factory- and user-trip point options
- Programmable hysteresis options
- Dual trip point options

Fan Control and Management – EMC2XXX Family

- Temperature proportional fan speed control
- FanSense technology protects against fan and system failure
- Open-loop and closed-loop fan controllers



Thermocouple Sensor Conditioning

Thermocouple interfacing requires expertise in sensitive analog design, mixed-signal and high-order mathematics for realizing temperature from the small voltage (µV) output of a thermocouple. Microchip's Fully Integrated Thermocouple Electromotive Force (EMF) to Degree Celsius converter with cold-junction compensation greatly simplifies the design process by integrating all needed functions in one package, reducing time to market.

Target Applications

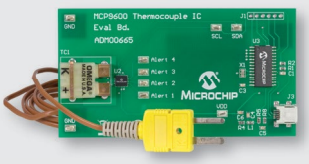
- Process control
- Boilers
- Water heaters
- Engine thermal monitoring
- Heating racks

Featured Product: MCP9600

Fully Integrated Thermocouple EMF to Degree Celsius Converter

- Supports eight thermocouple types: K, J, T, N, S, E, B and R
- ±1.5°C accuracy (max.)
- Integrated cold-junction compensation

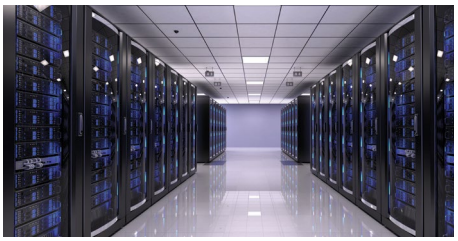
MCP9600 Thermocouple EMF to C Converter (ADM00665)



The MCP9600 Evaluation Board is available to enable you to easily evaluate the features of the MCP9600 Thermocouple EMF to Degree Celsius Converter using a Type K thermocouple. The device also supports Types J, T, N, E, B, S and R which can be evaluated by replacing the Type K Thermocouple connector with the corresponding connectors.

www.microchip.com/thermalmanagement

DC Current/Power Measurement



As the needs for energy efficiency and system reliability continue to grow, measurement of system currents and temperatures are becoming a necessity. Microchip's high side current sensors provide accurate current measurement, integrated ambient temperature sensors, remote diode sensing as well as system alert capability.

	EMC1701	EMC1702	EMC1704	PAC1710	PAC1720	PAC1921
Current Sensors	1	1	1	1	2	1
Common-Mode Voltage Range	3–24V	3–24V	3–24V	0–40V	0–40V	0–32V
FSR (±, mV)	10, 20, 40, 80	10, 20, 40, 80	10, 20, 40, 80	10, 20, 40, 80	10, 20, 40, 80	100
Temp. Sensors	1	2	4	–	–	–
Alert & Therm.	✓	✓	✓	✓	✓	✓
Peak Detect Pins	✓	✓	✓	–	–	–
Special Features	Bi-directional	Bi-directional	Bi-directional	Bi-directional	Bi-directional	Configurable Analog Output
Interface	2-wire/I²C compatible	2-wire/I²C compatible	2-wire/I²C compatible	2-wire/I²C compatible	2-wire/I²C compatible	2-wire/I²C compatible
Package	12-pin 4 × 4 QFN, 10-pin MSOP	12-pin 4 × 4 QFN	16-pin 4 × 4 QFN, 14-pin SOIC	10-pin MSOP	10-pin MSOP	10-pin VDFN

Featured Product: PAC1921

The world's first high-side current/power sensor with 2-wire bus and configurable analog output

- Configurable measurement type output: power, current or bus voltage
- Configurable voltage output (3V, 2V, 1.5V, 1V)
- 100 mV full-scale current sense voltage range
- Second-order delta-sigma ADC with 11-bit or 14-bit resolution
- 1% power measurement accuracy
- Auto-zero offset
- Auto sleep state: automatically shifts to low-power state (3.5 µA)
- V_{DD} = 3.3V nominal (operational range 3.0V to 5.5V)
- Bus range: 0V to 32V
- No input filters required

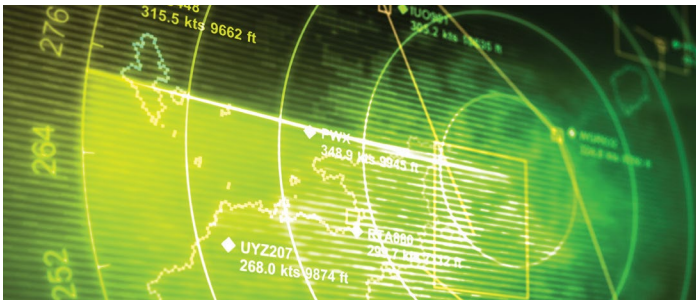
PAC1921 High-Side Power and Current Monitor Evaluation Board (ADM00592)

The PAC1921 is a dedicated power monitoring device with a configurable analog output. This device is unique in that all power related information is available on the 2-wire/I²C-compatible interface and power, current or voltage is available on the analog output. The PAC1921 High-Side Current/Power Sensor Evaluation Board provides you with the means to exercise device functionality while connected either to target systems (Sys Mode) or while utilizing on-board sources (Demo Mode).

Data Acquisition Solutions

High-Speed Data Acquisition

Offering sampling speeds up to 200 Msps and low-power operation of less than 500 mW, Microchip's pipelined 12-/14-/16-bit resolution ADCs are ideal for low-power, space-constrained portable data acquisition applications. The integrated decimation filters and down converter reduces the need for external RF circuitry and external signal processing, further saving power and board space.



Target Applications

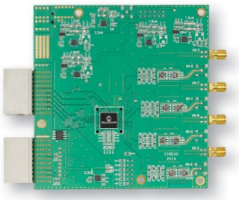
- Radar
- Ultrasound
- Software-defined radios
- Sonar imaging
- Portable data acquisition

Featured Product: MCP37D31-200

200 Msps, 16-bit ADC with Advanced Integrated Features

- Power-saving CMOS design
- On-board decimation filtering
- Integrated digital down converter

MCP37X3X-200 16-bit 200 Msps ADC VTLA Evaluation Board (ADM00505)



The MCP37X3X-200 16-bit 200 Msps ADC VTLA Evaluation Board enables you to evaluate the performance and digital signal processing features of the MCP37X3X-200 family of 16-bit, 200 Msps pipelined ADCs. It is used with a compatible data capture card to allow you to access the performance analysis features via a graphic user interface that runs on your PC.

High-Resolution Precision Data Acquisition

Delta-sigma ADC families offer 16 to 24 bits of resolution with sampling rates from 4 sps to over 100 ksps. Family features include low-power operation, low output noise and choices of I^2C and SPI interfaces. High integration, including on-board voltage references and Programmable Gain Amplifiers (PGAs), as well as small packaging such as SOT-23 and DFN, allow for high-density solutions.

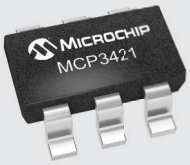
Target Applications

- Portable instrumentation
- Weigh scales
- Temperature-sensing applications with RTD, thermistor and thermocouple
- Bridge sensing: pressure, strain and force

Featured Product: MCP3421

18-bit Delta-Sigma ADC

- Space-saving 6-pin SOT-23 packaging
- On-board reference and PGA
- 145 µA low current operation



MCP3421 Weight Scale Demonstration Board (MCP3421DM-WS)

This demonstration board is designed to evaluate the performance of the low power consumption, 18-bit ADC in an electronic weight scale design. Next to the MCP3421 there is a low-noise, auto-zero MCP6V07 op amp. This can be used to investigate the impact of extra gain added before the ADC for performance improvement. A PIC18F4550 MCU controls the LCD and the USB communication with the PC. The GUI is used to indicate the performance parameters of the design and for calibration of the weight scale.

Energy Measurement

Microchip's Energy Measurement products enable accurate measurement of energy for electricity metering and power monitoring applications. The MCP39FXX offers on-chip power calculations and high-end AFEs for high-accuracy measurement, and the accompanying firmware performs the power calculations on our PIC® microcontrollers.

Feature	MCP39F511N	MCP39F521	MCP39F511	MCP39F501
Inputs	1 Voltage 2 Current	1 Voltage 1 Current	1 Voltage 1 Current	1 Voltage 1 Current
Energy Accumulation	✓	✓	✓	–
Event Monitoring	6	4	5	8
Zero-Crossing Detection	✓	✓	✓	–
PWM Output	✓	–	✓	–
Min/Max Values Tracking	✓	✓	✓	–
Multiple Device on Bus	–	✓	–	✓
Interface	UART: Selectable	I²C: 400 kHz	UART: Selectable	UART: 4.8 kbps
Single-Wire Output	–	–	✓	✓

Target Applications

- Smart plugs
- Power monitoring for home automation
- Smart lighting
- Real-time input power measurement of AC/DC power supplies
- Intelligent power distribution units
- Power meters

MCP39F511N Power Monitor Demonstration Board (ADM00706)

This demonstration board is a fully functional single-phase, dual-load power monitor which demonstrates the features of the MCP39F511N Power Monitoring IC. The MCP39F511N calculates active power, reactive power, accumulated energy and RMS current for two current channels, as well as RMS voltage and line frequency, plus additional features useful to power monitoring designs.

www.microchip.com/dataconverters

Sensors and Security

RE46C317/18: Piezoelectric Horn Driver with Boost Converter

The RE46C317 is a Complimentary Metal-Oxide Semiconductor (CMOS) piezoelectric horn driver IC with built-in boost converter. It is intended for use in 3V battery or battery-backed applications. The circuit features a DC-to-DC boost converter and a driver circuit suitable for driving a piezoelectric horn. The RE46C317 is compatible with the RE46C117 and offers lower standby current. The RE46C317 provides a tri-state input for horn enable.

Features

- 3V operation
- Low quiescent current
- 10V on-board boost converter
- Low horn driver on resistance

Applications

- Smoke detectors
- CO detectors
- Personal security products
- Electronic toys

Flexible, Configurable Power Control

Digitally Enhanced Power Analog (DEPA) technology from Microchip combines the power and performance of an analog-based controller with the flexibility of a digital interface, offering an industry-leading level of configurability. DEPA technology allows the user to configure many operating parameters "on-the-fly", including output voltage, current limit, UVLO, MOSFET drive and compensation, providing maximum flexibility.

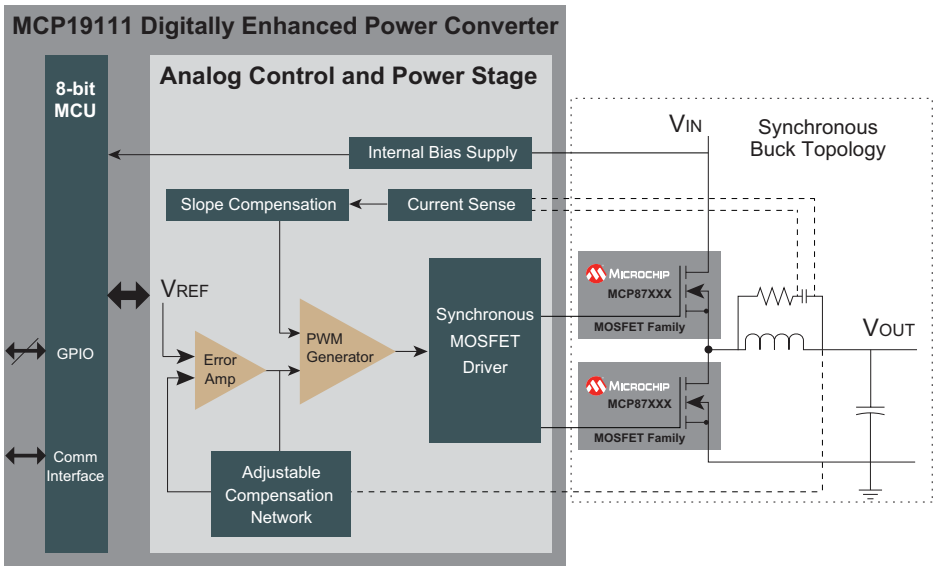
Features

- Fast transient response analog control loop
- Integrated 8-bit PIC® MCUs provides significant configurability
- PMBus™/I²C communication interface
- Integrated MOSFET drivers, current sense and adjustable compensation
- MPLAB® X Integrated Development Environment (IDE) support: GUI configurable

Target Applications

- LED lighting
- DC-DC point of load
- Battery charging
- Networking/server applications

Hybrid Control (Analog + Digital)

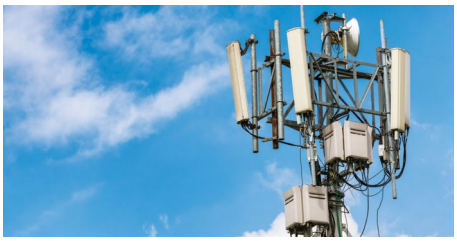


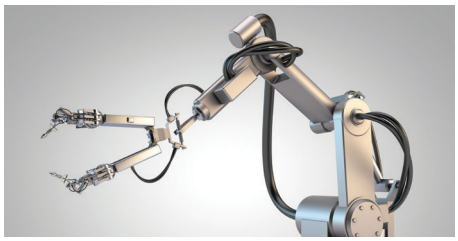
Hybrid PWM Controllers

Product	Input Voltage Range (V)	Output Voltage (V)	Operating Temp. Range (°C)	Topologies Supported	Program Memory Size (kWords)	RAM (bytes)	Packages
MCP19110	4.5 to 32	90% of VIN	–40 to +125	Buck	4	256	28-pin 4 × 4 QFN
MCP19111	4.5 to 32	90% of VIN	–40 to +125	Buck	4	256	24-pin 5 × 5 QFN
MCP19114	4.5 to 42	0.5 of VIN (dependent on topology)	–40 to +125	Boost, Flyback, SEPIC, Ćuk	4	256	24-pin 4 × 4 QFN
MCP19115	4.5 to 42	0.5 of VIN (dependent on topology)	–40 to +125	Boost, Flyback, SEPIC, Ćuk	4	256	28-pin 5 × 5 QFN
MCP19116	4.5 to 42	0.5 of VIN (dependent on topology)	–40 to +125	Boost, Flyback, SEPIC, Ćuk	8	336	24-pin 4 × 4 QFN
MCP19117	4.5 to 42	0.5 of VIN (dependent on topology)	–40 to +125	Boost, Flyback, SEPIC, Ćuk	8	336	28-pin 5 × 5 QFN
MCP19118	4.5 to 40	0.5 to 90% of VIN	–40 to +125	Buck	4	256	24-pin 4 × 4 QFN
MCP19119	4.5 to 40	0.5 to 90% of VIN	–40 to +125	Buck	4	256	28-pin 5 × 5 QFN

www.microchip.com/DEPA

High-Density Fully Integrated Power Modules





Highly integrated power module solutions are designed to simplify power system design by offering a complete switching DC-DC converter solution in an ultra-compact, thermally enhanced, rugged QFN package. These modules integrate a PWM controller, power MOSFETs, inductor and associated discrete passive components to save board space and reduce component count, resulting in higher system reliability.

Features

- Ease of use (no external inductor required)
  - Turnkey solution for fast time to market
  - Integrated controller, inductor and MOSFETs
  - Easy layout and assembly
- Small form factor
  - Small QFN package reduces solution size
  - Up to 60% smaller than discrete solutions
- High performance
  - Up to 93% peak efficiency
  - Low radiated emission (EMI) meets CISPR22, Class-B
  - Hyper Speed Control® architecture enables fast load transient response
  - HyperLight Load® mode improves light load efficiency
- Robust
  - Few external components improve reliability
  - Rugged package design for enhanced thermal performance, vibration and humidity resistance
  - Specified from –40°C to +125°C

Simple and Small Footprint

MIC45404 fully integrated power module

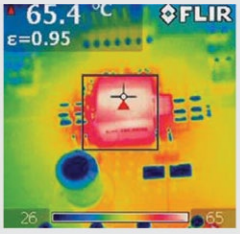
- Simple to use with pin programmability
- Small 10 × 6 mm QFN package with ultra-low 2 mm package height

MIC45404 Evaluation Board (MIC45404YMP-EV)

- 19V, 5A DC-DC power module

Superior Thermal Performance

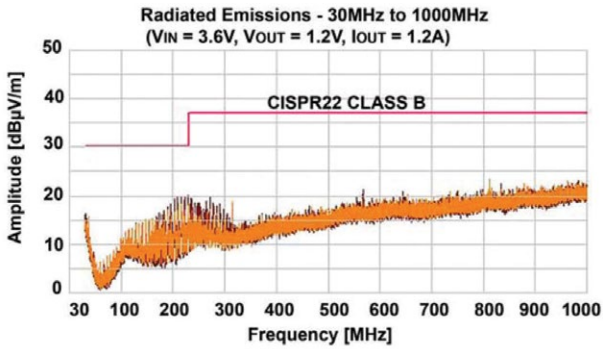
MIC45212, V_{IN} = 12V, V_{OUT} = 1.2V, f = 600 kHz, I_{OUT} = 10A, T_A = 25°C



Featured Products

	400 mA	600 mA	1A	1.2A	2A	3A	5A	6A	10A	14A
4.5–70V	–	–	–	–	–	MIC28304	–	–	–	–
4.5–26V	–	–	–	–	–	–	MIC45404	MIC45205	MIC45208	MIC45212
2.7–5.5V	MIC33030	MIC33050	MIC33163	MIC33153	MIC33263	–	–	–	–	–

Meets EMI Requirements

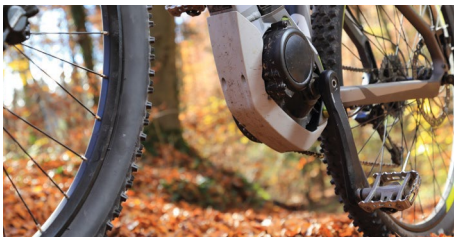


Target Applications

- Telecom
- Network switches and routers
- Server storage
- DC power distribution
- Industrial
- Solid state drives

www.microchip.com/powermanagement

Motor and MOSFET Drive



Motor drivers and MOSFET drivers address a wide range of applications including appliances, automotive, power tools, medical equipment and industrial equipment, to name just a few. Microchip offers three families of driver solutions: fully integrated, companion and discrete gate drivers. Singles, duals and quads, with voltage capability from 6V to 600V and current drive capability from 500 mA to 12A are available, and offer valuable features including enable pins, inverting, non-inverting and complementary outputs, anti-shoot through and adaptive dead-time technology.

Full Integrated Solutions (Integrated MOSFETs)

Dual H-Bridge Motor Driver

- 10V to 40V
- 750 mA output
- Drive both windings of stepper motors

3-Phase Motor Drivers

- 2V to 14V
- 800 mA to 1.5A output
- 180° sinusoidal drive

Companion Solutions

3-Phase BLDC Gate Drivers

- 6V to 28V
- Load dump protection
- Integrated op amps
- Integrated DC/DC regulators
- Over-current protection

Discrete Solutions

MOSFET Drivers

- 5V to 600V
- 0.5A to 12A
- Anti-shoot-through
- Adaptive dead-time
- Enable pins

Featured Products

MIC4606: 85V Full-Bridge FET Drivers

- 5.5 V to 16V gate drive supply voltage rating
- Advanced adaptive dead-time
- Intelligent shoot-through protection

Target Applications

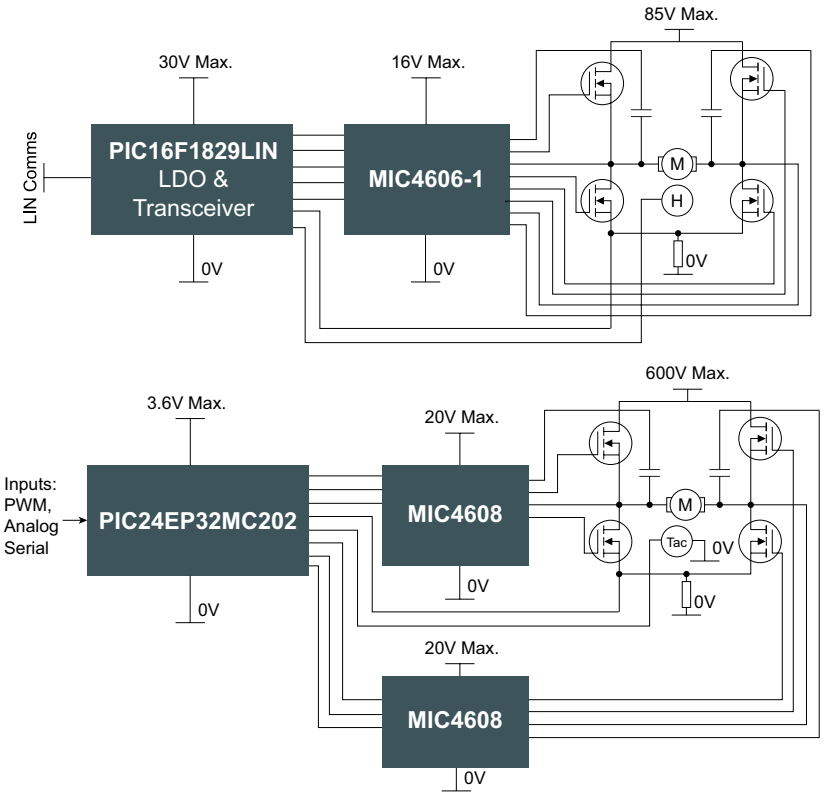
- Full-bridge motor drives
- Automotive
- Stepper motors

MIC4608: 600V Half-Bridge IGBT or MOSFET Driver

- 10V to 20V gate driver supply voltage rating
- Independent input or single PWM input signal
- Shoot through protection

Target Applications

- Full- and half-bridge motor driver
- Industrial controls
- White goods



www.microchip.com/motordrivers

High-Performance Low Dropout (LDO) Solutions

Microchip's family of low dropout linear regulators provide you with a wide variety of solutions including ultra-small packaging, high output current and high input voltage capability, low quiescent current and low-noise performance.

Features

- *Better Efficiency* – enhance the efficiency by providing lower quiescent current (I_Q) and lower dropouts across the input and output. Target applications include always-on devices, camera modules, low-output-voltage core power supply applications and low-power sensors.
- *Smaller Solution Size* – minimize solution size by providing capless LDOs and multiple output (combo) LDOs. Target applications include touch screens, LCD controllers, camera modules, ICs requiring multiple power rails and sensors.
- *Noise Performance* – enhance the noise performance by providing high PSRR, ultra-low output noise and fast transient response. Target applications include camera sensors, audio DSPs, Bluetooth®, wireless transceivers and noise-sensitive mixed-signal ICs.

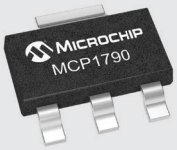
Low Noise (RF Applications)

MCP1790 and MCP1791

- High PSRR of 90 dB @ 100 Hz

MIC943XX Family (Ripple Blocker™ Technology)

- >60 dB PSRR @ 40 kHz to 5MHz



Automotive/Industrial

MIC528X Series, MAQ528X (Automotive)

- Input voltage up to 120V

MIC2975X Series

- Output current up to 7.5A

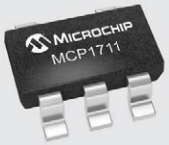
Portable Equipment

MCP1711

- Capless LDO, 1 × 1 mm DFN

MCP5501/2/3/4

- 300 mA, 1 × 1 mm DFN

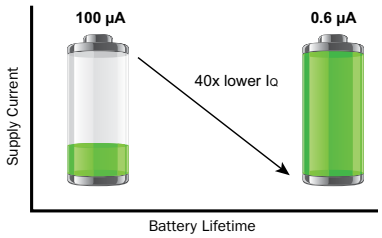


Battery-Powered Equipment

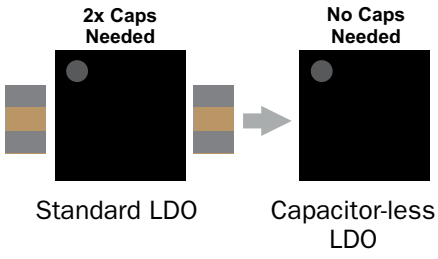
MCP1703A

- Low I_Q of 2 µA
- Wide input voltage up to 16V

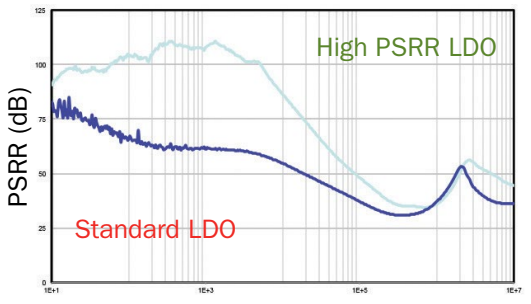
Ultra-Low I_Q (<1 µA)



Capless Operation



Ultra-High Ripple Rejection (<90 dB)



High-Efficiency DC-DC Voltage Regulation

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Target Applications

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- Communication/networking
- Industrial power

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Target Applications

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Target Applications

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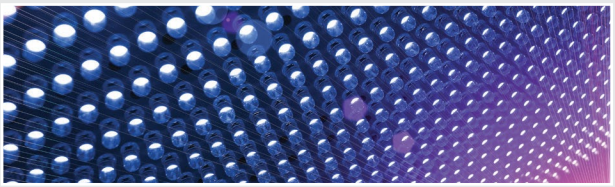

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Target Applications

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Typical Applications

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- Agriculture
- Healthcare
- Communication

Featured CAN Products

Product	CAN Type	Feature	Description	Packages
MCP2561	High-Speed	Split Pin	Common mode stabilization	8-pin PDIP, SOIC, DFN (3 × 3 mm)
MCP2562	High-Speed	VIO Pin	Internal level shifter on digital I/O pins	8-pin PDIP, SOIC, DFN (3 × 3 mm)
MCP2561FD	Flexible Data Rate	Split Pin	Common mode stabilization	8-pin PDIP, SOIC, DFN (3 × 3 mm)
MCP2562FD	Flexible Data Rate	VIO Pin	Internal level shifter on digital I/O pins	8-pin PDIP, SOIC, DFN (3 × 3 mm)

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Transceiver Features

- Compliant with LIN 2.1 and SAEJ2602
- Approved by OEMs globally
- Industry-leading ESD/EMC performance
- Sleep mode < 5 µA
- Extremely low current consumption

Target Applications

- Body control
- Intelligent sensors and switches
- Energy management

Featured LIN Products

Microchip Solution	Level of Integration	Suggested Products	Description
LIN Transceiver	Low	MCP200X Family	Stand-alone LIN transceiver family
	Medium	MCP202XA Family	LIN transceiver family with integrated voltage regulator
		MCP2050	LIN transceiver with integrated voltage regulator and windowed watchdog timer
Voltage Regulator	Low	MCP179X Family	70 mA, high-voltage linear regulator family

www.microchip.com/LIN

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32K OLED resolution in demand for holographic smartphones

By Julien Happich

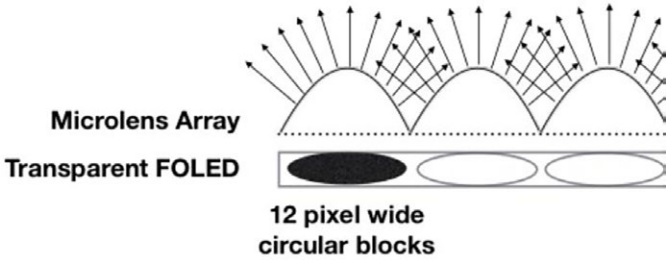
In their recent paper "HoloFlex: A Flexible Holographic Smartphone with Bend Input", researchers from Queen's University's Human Media Lab (Ontario, Canada) disclosed the world's first holographic smartphone.

The researchers laminated a flexible micro-lens array on top of the OLED-based ReFlex flexible smartphone they had demonstrated back in February to turn its bendable touch-display into a light-field capable interface. Combined with custom ray-tracing algorithms running on the phone's GPU, the flexible display renders holographic-like 3D images with motion parallax and stereoscopy to multiple simultaneous users without head tracking or glasses.

For this prototype, the researchers used 3D-printing to fabricate a matrix of 16,000 fish-eye lenses (only 0.75mm wide each) and cover a 1920x1080 full high-definition OLED display with it (403dpi with about a 0.063mm pixel pitch). Since each micro-lens dome covers 12-pixel wide sub-images (in fact a circular image made of approximately 80 pixels), they each contribute a pixel block of the entire scene from a particular virtual camera position with a 35° field of view (determined by the optical properties of the micro-lenses). Altogether, this yields a 160x104 resolution image floating in 3D a few centimetres off the actual screen, to be viewed from any angle.

As for the ReFlex smartphone, touch input allows for x,y input, while bend sensors allow users to control the z dimension, by squeezing the display.

Since the final image is accumulative of the many rays from the light-field display (and the sub-image resolution under each micro-lens), at what sort of OLED screen resolutions would the image quality become visually acceptable for OEMs and consumers to adopt such holographic displays? We asked Dr. Roel Vertegaal, Professor of Human-Computer Interaction at Queen's University's School of Computing in Kingston, Ontario, and director of the Human Media Laboratory.



HoloFlex side close-up with 12-pixel wide pixel blocks and half-dome microlens array dispersing light rays.

"I think when mobile displays reach 16K or 32K and a pixel pitch of 4 to 2 microns the quality would be similar to what we are used to today in 2D screens", Vertegaal wrote *EETimes Europe*.

That's orders of magnitude the resolution of today's top of the range Ultra HD 4K smartphones (3840x2160 pixels), not even a mainstream feature, but some micro-OLED manufacturers are nearing such pixel pitches (at undisclosed yields).

With higher native screen resolutions, the micro-lens could not only be shrunk, but each dome may also pack more pixel information (finer sub-images) for a better rendering. The micro-lens array has still plenty of scope to be shrunk, using nano-imprint technologies for example.

"The current size of the micro-lenses is about 12 pixels across which is acceptable for 3D content that is within 1-2 cm depth-wise of the display. I think a commercial product might double that (which would conversely double the required resolution I mentioned earlier", Vertegaal clarified.

"I think the two main limiting factors today (provided we can make the micro-lens array as small as needed) are screen resolution and GPU architecture and power. As mentioned in our paper the 3D content is rendered using a ray tracing algorithm which is computationally expensive and hardware support for ray tracing in mobile GPUs would be nice", he continued.

When asked if the technology would become licensable IP through Immersion Inc., a backer of this research, or if the professor would conceive establishing a startup to commercialize the solution together with display OEMs, Vertegaal eluded the question.

"We did patent the device but cannot comment on further commercialisations activity", he answered.

Providing OLEDs reach the required pixel pitch, example applications could be to use the bend gestures of the HoloFlex for Z-Input to facilitate the editing of 3D models, swiping the screen to manipulate objects in the x and y axes while squeezing the display to move objects along the z-axis.

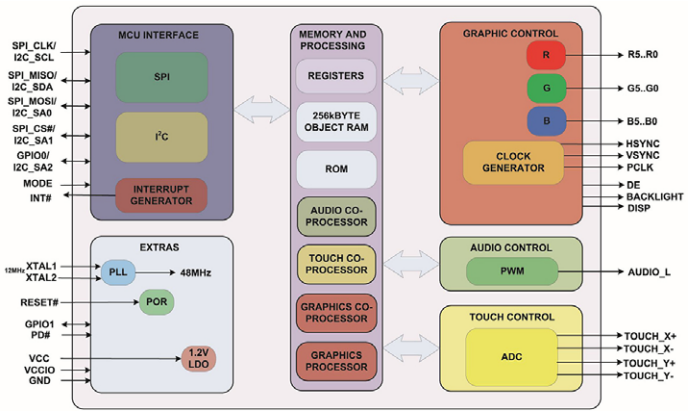
Combined with a depth camera, users could also indulge in holographic video conferences with one another, envisions Dr. Vertegaal. Holographic gaming is another promising application, in fact, the researchers rendered a 3D version of Angry Birds, where bending the side of the display would pull the elastic rubber band that propels the bird. Sending the bird to fly over the screen, in the third dimension.

Bring touch technology to existing designs with FTDI's embedded video engine

By Mark Patrick

When the Apple iPhone was launched almost a decade ago it triggered a revolution in the design of user interfaces for embedded systems. Although touchscreens had been in use for several decades before then in systems ranging from computer-aided design terminals to advanced industrial controls, the incorporation of gestures into the man-machine interfaces demonstrated many new possibilities for interaction.

Users found the idea of using touch together with pinch and zoom gestures easy to grasp and have quickly come to demand capabilities from many of the other systems with which they interact. That in turn drives the need for manufacturers of a wide range of systems to upgrade the user interfaces on their products. The traditional combination of buttons and simple seven-segment LCD or LED indicators can put a product at a disadvantage in the market to one that displays animated graphics and which can overlay helpful hints and other explanatory text.



FT800 block diagram

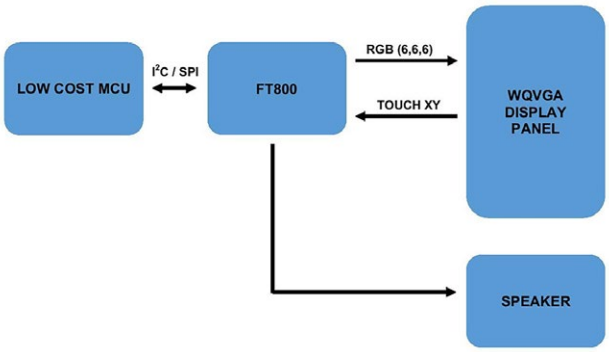
As touch panel costs have fallen in response to market demand, the LCD-based interface can provide cost advantages to the manufacturer. Simple firmware changes or register settings can be used to fully localise a product, removing the need to screen-print different languages onto panels that contain physical knobs and buttons. The savings in inventory can lead to major improvements in business efficiency.

Although there are advantages to moving to a touch-based interface from a traditional design based on mechanical controls and simpler displays, the design changes could have major repercussions on the core system architecture.

The move from a simple seven-segment LCD and a button matrix to a fully graphical touchscreen represents a major shift in the processing power needed and, potentially, major and costly changes to the core software. If the graphics are to run on a single processor, they will likely demand the use of a 32bit processor in order to be able to write to a high-resolution framebuffer. Without complicated paging and segmentation schemes, a system implemented on an 8bit or 16bit microcontroller will not be able to write to the full framebuffer's address range or have enough space for sophisticated graphics.

Although the market price of 32bit graphics-capable processors has fallen in recent year, the time and cost needed to alter the application and then requalify and test it could prove prohibitive. However, there is a way to add a highly capable touchscreen interface to an existing application that may run on a comparatively simple, resource-limited microcontroller that does not involve extensive rework. The FTDI Chip Embedded Video Engine (EVE) is a family of integrated circuits (IC) designed to handle interactions with LCD-based touchscreens on behalf of a host microcontroller.

The EVE technology takes advantage of the model-view-controller (MVC) software architectural pattern developed for the first graphical user interfaces (GUIs) at Xerox Palo Alto Research Center. The MVC pattern divides the application into three interconnected parts. The model manages the data and rules of the core application. The view portion presents information to the user, deriving it from updates provided by the model component. The controller portion interprets inputs from the user and converts them into commands that the model can apply to its internal logic.

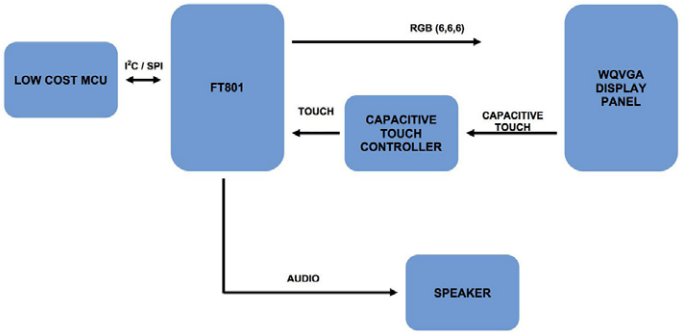


System architecture for a resistive touchscreen

The separation of functions in MVC makes it possible to use the same core logic to drive different types of user interface. An existing user interface based on a keypad and seven-segment display might use a pair of buttons to let the user scroll through several pages of text and command options. A version based on a capacitive touchscreen may use swipe gestures familiar to tablet and smartphone users to move through the pages. Though the user interaction is different, the core logic that needs to be processed by the model part of the application remains the same – it is responding to page-forward and page-backward commands.

Using a simple SPI or I2C serial interface, the EVE can relay the necessary commands to the model logic that runs inside the host microcontroller. The result is that the core application can, for the most part, continue to run with the new interface with minimal changes. Most of the changes needed to deal with the GUI and touch behaviour are incorporated instead into the EVE controller.

Mark Patrick is supplier marketing manager, EMEA at Mouser Electronics - www.mouser.com



System architecture for a capacitive touchscreen

The EVE technology is not restricted to capacitive touch. The FT800 devices support resistive touch screens that are often used in harsh environments and where low system cost is important. The FT800 provides a direct connection for the x and y inputs from the touchscreen controller, converting touch input into commands that the host microcontroller can understand.

The FT801 devices support an interface to an external capacitive touch controller that is typically integrated into the LCD panel assembly. For high compatibility with the existing user interface code, the FT801 offers a single-touch mode that mimics conventional button presses. The extended mode supports multi-touch operation with up to five touch points, allowing the support of pinch and zoom gestures and other more complex gestures. For example, in a system that presents images to the user, they may use the zoom and pinch gestures to look at different parts of the picture.

To define and control the GUI, the application in the host microcontroller performs some of the view functions of the MVC design pattern. Typically, the application will call on objects loaded into the EVE's memory using display lists. The display lists let the application call up different bitmaps and have them rendered on screen or draw graphs and other vector images using commands to draw lines and other primitives. The display-list technique minimises memory usage in the host microcontroller as each individual drawing command is just 4byte in length.

The graphics themselves are built with the help of a screen editor that runs under Windows. Using drag-and-drop techniques, the screen editor constructs the display lists that will be manipulated in real time by the microcontroller to form the GUI. An emulator library makes it easy to demonstrate GUIs and map graphics from other tools into the EVE environment.

A coprocessor element in the EVE allows the manipulation of more advanced graphic elements, such as widgets and the touch tags needed for multi-touch operation. Widgets make it easier to combine bitmaps with animated graphics without demanding the host microcontroller perform the graphics operations directly. For example, a built-in clock command will overlay a moving hand over a background bitmap. A similar function provides an easy-to-use speed-indicator or fuel-gauge widget.

By taking into account the problems faced by manufacturers when making the switch from traditional user interfaces to a touch-based solution, the EVE family of ICs from FTDI Chip provides a much smoother migration path than the conventional approach that would, in most cases, rely on a major upgrade to the system's core microcontroller. Leveraging the MVC design pattern, commands and data relayed over a serial connection make it possible for even low-end microcontrollers to drive GUIs with smooth, animated graphics and process touch gestures.

Memory in Pixel: a superior display technology for e-bikes

By Marco Meier

The electrification of personal transportation is well underway in Europe. Adoption has soared. Double-digit growth is forecast to continue for the foreseeable future. Most of these electrified vehicles are "pedelecs," a term derived from pedaled electric bicycles. E-bikes, as they are also known, flatten out hills with battery-powered assistance. Yet despite their advanced technology, they still look very similar to conventional bicycles. That makes it easy to forget important considerations such as display quality when buying an e-bike.

Sharp Devices Europe, Thinkstock.

Easy to pedal, difficult to choose

E-bikes are still a relatively new product category. Consumers are frequently left scratching their heads when it's time to choose a model. It doesn't help that the technology used in e-bikes is becoming more sophisticated all the time. An on-board computer is practically standard equipment these days. Riders enjoy a wide range of capabilities ranging from maps, navigation, and heart rate to range information.

These useful features generally have one thing in common on every e-bike — they rely on its user interface. That means you'll find a display of some sort mounted to the handlebars. But not all displays are created equal.

The computer display is easily overlooked by consumers accustomed to purchasing conventional bicycles. But it's an essential component of any e-bike, and a great place to start when selecting your next pedelec. Because without a readable user interface, you may not be able to use the advanced features you've paid for. With some basic knowledge of the available technologies, consumers can quickly narrow down their choices and make a better decision.

Marco Meier is Key Account Manager at Sharp Devices Europe - www.sharpsde.com

Humble beginnings

The first generation of e-bikes was quite simple, often lacking a digital display of any kind. Early models used an arrangement of just three LEDs to indicate the battery's level of charge. But the simple three-LED gauges common in the early days of electric bicycles were not always easy to read in sunshine. Now, that functionality is integrated into the e-bike's on-board computer. It offers information similar to what conventional aftermarket cycling computers provide. That often includes road speed, distance travelled, and even the rider's heart rate.

The introduction of seven-segment FSTN LCD displays — the type found in digital clocks, calculators, and in-store price displays — represented a step up from basic LED indicators. One drawback of FSTN technology however is its comparably high power consumption. And here as well, the amount and type of information that can be displayed is limited because of the low contrast and inability to display graphics.

You can't just phone it in

Now let's move from very basic displays to high-end solutions for e-bikes. At this end of the spectrum, we have full-colour, backlit TN LCDs and OLED displays. You'll find screens based on these technologies in most modern PCs, tablets, and smartphones. They are capable of displaying brilliant colours, animations, and crisp video. But they have considerable drawbacks when used in cycling computers, which often push these displays to their limits — especially in bright outdoor riding conditions.

Nothing to see here

The most critical flaw of technologies that rely on a backlight is their poor contrast and readability in direct sunlight. To increase the contrast of a TN or OLED panel for better readability in bright ambient conditions, a dramatic increase in backlight brightness is required. Instead of using the sun's light to their advantage, these types of displays actually try to compete

with it. Anyone who has turned on a flashlight outside on a sunny day knows that's a losing proposition. Even worse, the brighter the ambient lighting conditions, the more power these displays consume. When you're relying on a battery to get you from point A to point B, every little bit counts. And for normal bicycles or retrofit e-bike computers, these types of displays cannot be operated using disposable coin cells.

It's dangerous to allow the brilliant display of your full-colour smartphone to distract you while driving an automobile. That's a well-established fact. The same is of course true on a bicycle. Does that mean we should go back to the days of seven segment LCDs, or even crude LED indicators? Luckily, there are more sophisticated options that are easy to read in sunlight and don't involve a backlit TN panel.

Don't read and ride

You may be familiar with e-ink, the technology behind most popular ebook readers. It has an appearance similar to ink on paper. But e-ink displays have long refresh times and must briefly go blank before displaying the next frame. That disqualifies them for any application requiring fast screen refresh rates, such as maps or navigation. Even worse, every refresh of an e-ink display consumes a great deal of power. These issues disqualify e-ink as a viable cycling computer display technology.

Thankfully, more elegant solutions for outdoor use do exist. An excellent answer has been provided in the form of LCD displays that achieve high contrast levels by reflecting the sun's light. Such reflective and transflective displays shine brighter as the ambient light increases. A backlight is not required, but can be implemented if desired. Good contrast is retained even in direct sunlight.

The elephant in the room — a display that never forgets

A recent innovation from the Sharp Corporation has also dramatically increased the efficiency of small displays for static images while still offering crisp video and animation. Sharp calls its technology Memory in Pixel because they have integrated memory circuits into each individual dot on the screen. This single bit of memory allows static images to remain visible for long periods of time without a screen refresh.

Reflective Memory in Pixel (MiP) displays also offer excellent contrast and visibility both under direct sunlight and in low ambient light conditions, with or without a backlight. In the sun, reflective MiP displays require no backlight whatsoever. The sun's light itself is reflected back by the display for crisp contrast and easy readability. Unlike TN displays, a backlight is only required for viewing MiP displays in total darkness. That means they draw less power from your e-bike's battery.

But most of all, MiP displays deliver exceptional clarity and readability in all riding conditions. Taken together, the advantages of these efficient monochrome displays make them an excellent choice for any cycling computer, and a preferred solution for high-end e-bikes. What's more, they enable advanced features such as navigation, animations, other complex graphics without the power drain of conventional LCDs. That means you can have navigation and other useful apps while extending range and limiting distractions.

Software-defined development takes DSP to the next level

By Olivier Tremois

Digital Signal Processing is migrating into high-performance platform devices to satisfy demands for more intensive processing and increased system integration. A new software-defined development flow provides accessibility for embedded-software designers working entirely in C/C++.

Digital signal processing is a critical enabler for equipment and services that have become essential in today's world. These include telecom and networking, mobile communications, digital audio, streaming video, industrial motor control and machine vision, automotive driver assistance, high-performance radar, and government signals intelligence.

To satisfy demands for more sophisticated system capabilities, reduced latency and increased channel capacity, dedicated digital signal processor (DSPs) have evolved into multicore devices that offer throughput reaching tens of GFLOPS and can be used as a single DSP or in a large multi-DSP board.

Still, the desire for further progress continues unabated, and today's equipment designers are also striving for greater system integration, lower component count, increased reliability and lower costs. To answer such demands, DSP extensions are now integrated in a variety of platforms, ranging from small embedded microcontrollers such as ARM® Cortex®-M4 devices to FPGAs and programmable System-on-Chip (SoC) ICs. These high-performance configurable devices have now become the designer's first choice when faced with intensive processing demands that can only be satisfied through a high degree of parallelism, or if the system requires high-performance interfaces or custom accelerators.

Emerging DSP platforms

Configurable SoCs integrate large numbers of DSP blocks with system functions including processors, memory, peripherals and programmable logic. The Xilinx Zynq-7000 series All-Programmable SoCs have up to 2,020 DSP slices, each containing a 25x8 multiplier, 48-bit accumulator and associated functions. Also on-chip are a Dual-core ARM Cortex-A9 MPCore application processing unit, standard high-speed peripherals such as USB 2.0 and Gigabit Ethernet, and dynamic memory interfaces such as LPDDR2 and DDR3.

On the other hand, the multi-processor Zynq MPSoC has additional resources including up to 3528 DSP slices built with a 27x18 multiplier, as well as extra PCIe Gen2, USB3.0, SATA 3.1 and DisplayPort peripherals, and support for DDR4 dynamic memory. The MPSoC architecture also integrates a dual-core ARM Cortex-R5 MPCore real-time processing core, a quad-core A53 as well as an ARM Mali-400 MP2 graphics processing unit (GPU) and H.264/H.265 video codec.

The Zynq-7000 and MPSoC high-performance ARM processors also benefit from tightly integrated NEON technology for multimedia acceleration, as well as FPGA DSP slices, integrated peripherals and up to 1,143,000 logic cells (in UltraScale+ MPSoCs). With these resources the devices provide the opportunity for highly parallel processing and extensive system integration beyond the capabilities of conventional multicore DSPs.

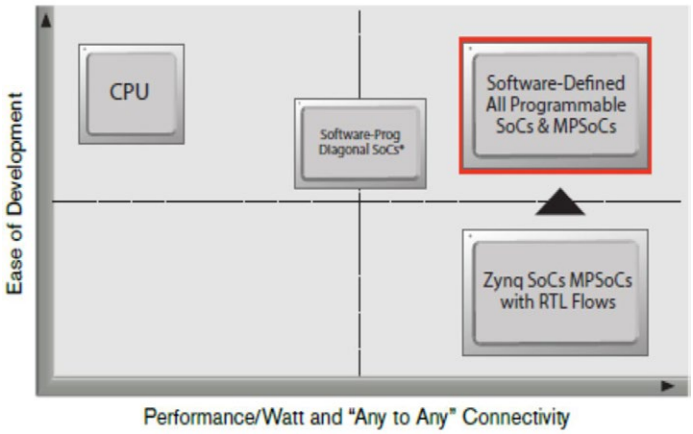


Fig 1: Software-defined flow allows embedded software developers to realise the performance potential of All Programmable SoC devices.

The time is right for designs teams currently pushing the performance limits of large multi-DSP boards to consider making the leap from conventional DSPs to an All Programmable SoC platform. Leveraging this technology, Xilinx engineers have recently helped one customer to redesign a radar board containing 32 conventional DSP chips, creating a new platform that contains just two field-programmable devices.

Hardware Synthesis at C/C++ level

Historically, designing with programmable FPGAs and SoCs has required engineers with hardware design skills to handle design work at the Register Transfer Level (RTL). This has discouraged predominantly software-skilled design teams from taking advantage of the extra capabilities and integration on offer. Figure 1 presents a graphical expression of the trade-off between ease of software development versus efficiency and flexibility. The diagram compares conventional software-programmable processors with programmable devices programmed at register-transfer (RTL) level or using a software-defined design flow.

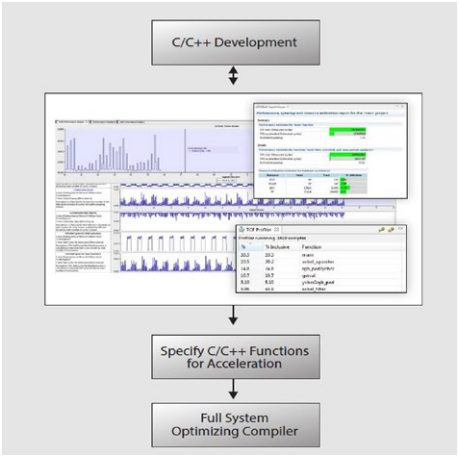


Fig. 2: The non-intrusive profiler is based on PC sampling.

Designing a traditional DSP-based solution has been perceived as a safe approach. However,

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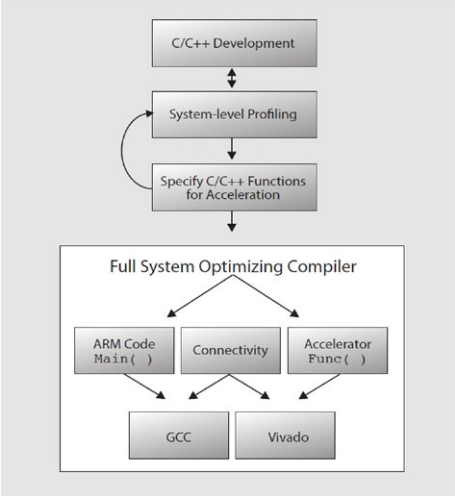

Fig. 3: The full-system compiler gives control over performance, throughput and latency, and ensures short design-iteration times.

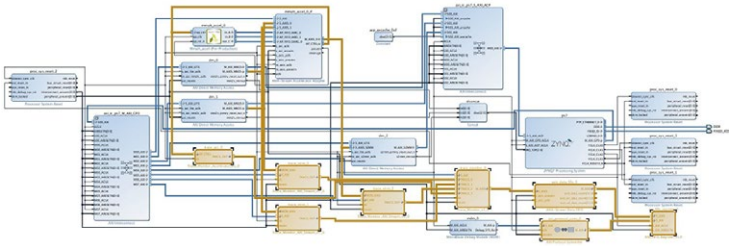

Fig. 4a: When enabled, SDoC Trace automatically inserts the necessary monitors and instrumentation.

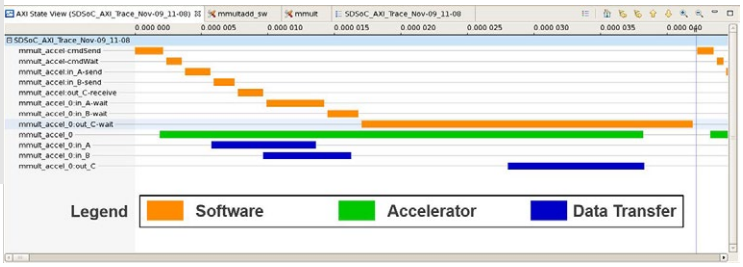

Fig. 4b: Trace visualisation shows the interplay between events in the hardware/software system.

as the demands of the highest performing applications continue to increase, and high-performance DSPs become more difficult to design with as a result of their multicore architectures, there is a clear need for a C/C++ design environment that delivers an ASSP-like programming experience to help systems and embedded-software engineers build multi-processing systems using All Programmable SoC ICs.

ASSP-like programming experience

Xilinx's SDSoC is an example of such a development environment, which allows software engineers to sit down and start developing C/C++ applications for programmable devices without needing to engage with traditional FPGA tools or Hardware Design Language (HDL).

It takes care of organising the on-chip processing and DSP resources, as well as programmable hardware and memory, to maximise system performance.

The environment incorporates a system-level profiler, which provides an early insight into overall system performance and power consumption. Figure 2 shows how the profiler fits into the SDSoC flow. The profiler quickly estimates system performance to help identify C/C++ functions that can be accelerated using programmable logic. SDSoC then instruments the code to report software cycles, estimate data-transfer times and monitor hardware utilisation such as cache, memory and bus utilisation.

This feature builds on the profiling capabilities of the established Xilinx SDK, which enables software-hardware performance measurement of a completed design running on a Zynq platform. Rapid estimation tools help users quickly assess the performance impact of moving one or more functions from software into hardware.

Enabling software developers to accelerate C/C++ functions independently in this way eliminates time-consuming interaction between hardware and software teams and helps minimise the number of iterations needed to take full advantage of programmable logic for software acceleration. The impact of any changes can be assessed within minutes, compared with several hours or more typically needed to generate actual hardware.

There is also a C/C++ full-system optimising compiler, which is the first tool of its type in the industry. It is capable of targeting the SoC's ARM processors as well as programmable logic and connectivity, as shown in figure 3. The compiler generates HDL code that is optimised for latency, bandwidth, and hardware utilisation. Together, the system-level profiler and system-optimising compiler can boost overall performance by a factor up to 100, compared to a software-centric solution without hardware acceleration.

System architects and platform developers with FPGA design expertise can take advantage of SDSoC to create optimised application platforms to hand-off to embedded-software developers.

With features such as automated system connectivity generation, this tool help architects work quickly to determine the optimal interconnect architecture between the Zynq processing system, memory and programmable logic-based accelerators.

In addition, architects can use SDSoC with Xilinx's Vivado design suite to create application-specific platforms, and to configure legacy FPGA IP such as RTL descriptions as C-callable libraries and thereby boost design productivity through reuse.

Hardware/software system-performance analysis

Engineers can see how their designs are performing in relation to workload, hardware/software partitioning, and system design choices by using SDSoC's tracing tool. SDSoC Trace gives a detailed view of system events that occur as the application is running, by tracing software running on the processor, hardware accelerators, and data transfer links in the system.

The events are presented graphically as a timeline view. Compared to event logging, tracing gives a view of the interactions between events over their duration and so gives deeper insights into application performance in a hardware/software system.

Figure 4 a shows how SDSoC Trace inserts monitors into the hardware system automatically. Tracing instrumentation is also inserted automatically in the software system. Figure 4b shows the hardware and software trace streams, highlighting the different types of events.

Support for board design

SDSoC enables software engineering to begin concurrently with the board-design effort leveraging Zynq All Programmable SoC-based development boards including the ZC702, ZC706, plus third-party and market-specific platforms including Zedboard, MicroZed, ZYBO, as well as Video and Imaging development kits. A Board Support Package (BSP) for each board is provided, and includes metadata that allows SDSoC to abstract the platform for embedded software developers and system architects, which helps further increase productivity and accelerate product development.

Powering FPGAs, ASICs and processors

By Mike Shriver

The current drawn by FPGAs, ASICs and processors for high performance servers, network and computing systems continues to rise, and load currents of 100A or greater are becoming common. Meanwhile, the chip's operating voltages are dropping to 0.9V and below with tighter voltage regulation requirements. For many of these applications, the core voltage may need to be adjusted for optimum performance with a VID (voltage identification) interface. A significant challenge is clearly placed on the power supply designer to meet the demands of high efficiency and tight output voltage regulation with a small amount of board space.

One way to meet these demands is to use the LTC3877 and LTC3874 chipset. The LTC3877 is a peak current mode, VID-controlled dual output synchronous step-down controller. The output of phase 1 can be programmed from 0.6V to 1.23V in 10mV increments with a six-bit parallel VID interface. Phase 2 provides an output of 0.6V to 5V, which is set by an external divider. The two phases can be paralleled together or with phases from another LTC3877 or an LTC3874 for higher output current.

The LTC3874 is a peak current mode phase extender chip. It does not have an error amplifier and instead regulates its phase current to the ITH signal from the LTC3877 master. The elegant design of the LTC3874 reduces trace count and board space. The LTC3877 comes in a 44-lead, 7x7mm QFN package; the LTC3874 slave controller comes in a 28-lead, 4x5mm QFN package.

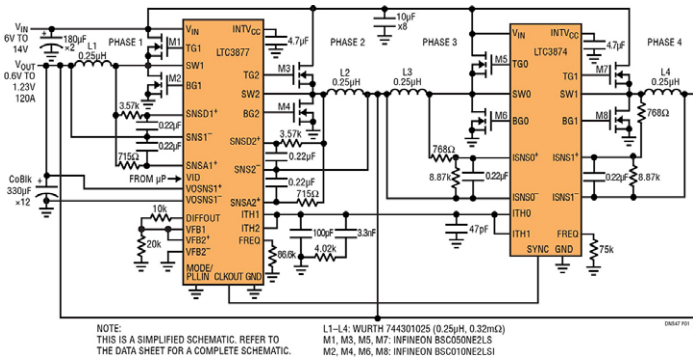

Fig. 1: 4-Phase 120A VID-controlled converter operating at a switching frequency of 400kHz

The 4-phase step-down converter shown in figure 1 uses the LTC3877 and LTC3874 to provide a VID-controlled output of 0.6V to 1.23V at a maximum load current of 120A at a switching frequency of 400kHz. The LTC3877 yields a total DC regulation accuracy of ±1% for all VID set points over temperature. The differential remote sense amplifier in the LTC3877 senses the output voltage at the regulation point and compensates for voltage drops across PCB trace runs and ground planes. The 4-phase operation results in lower output voltage ripple and faster load step response due to shorter clock delays.

High efficiency is a result of the strong gate drivers and short dead times of the two chips, MOSFET selection and sub-mΩ

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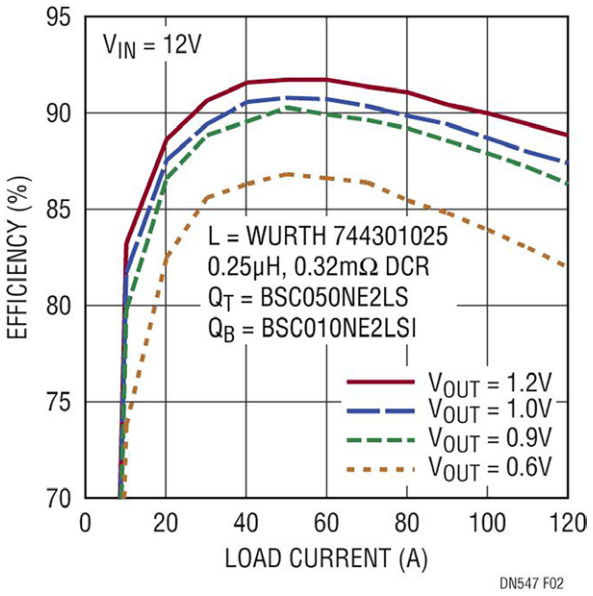


Fig. 2: Efficiency of the 4-phase 120A VID converter

DCR ferrite inductors. The full load efficiency for a 1.2V output at 120A load is 88.8% as shown in figure 2.

Sub-mΩ DCR sensing

Both the LTC3877 and LTC3874 use a proprietary DCR current sensing architecture designed for sub-mΩ DCR sensing, which ensures tight control of the current sharing and current limit. Figure 3 shows the current sharing performance of the 4-phase converter of figure 1. The inductor used is the Wurth 744301025 (250nH), which has a DCR of 0.32mΩ. The current sharing error is less than 1mV between phases.

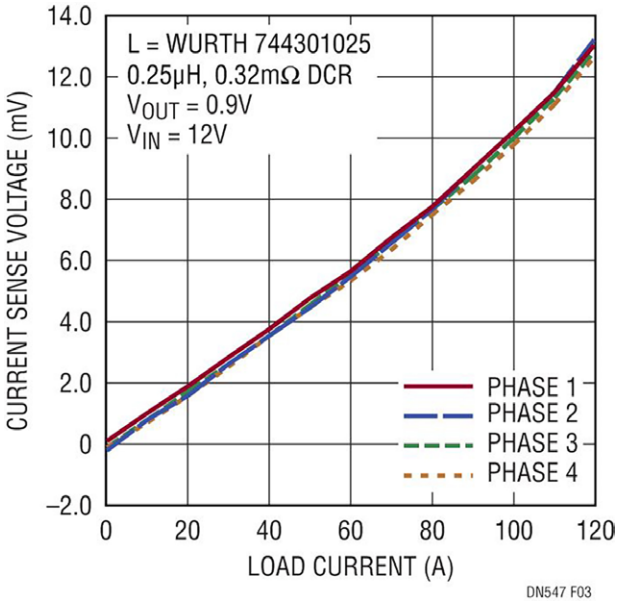


Fig. 3: Current sharing of the 4-phase 120A VID-controlled converter.

More features

The LTC3877 and LTC3874 both have a phase-lockable frequency range of 250kHz to 1MHz and a FREQ pin to set the internal frequency if synchronization is not required. The LTC3877 offers three light load operating modes: Burst Mode operation, forced continuous mode and pulse-skipping mode. The LTC3874 operates in either forced continuous mode or pulse-skipping mode.

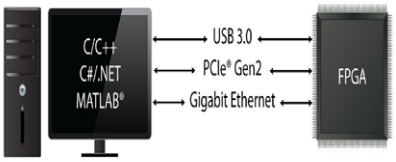
The minimum on-time of the LTC3877 is 40ns typical, ideal for high step-down converters or small footprint or high bandwidth converters operating at switching frequencies of 500kHz to 1MHz. The minimum on-time of the LTC3874 is 90ns, typical.

Phase 1 of the LTC3877 provides VID control. If the FPGA, ASIC or processor is not awake or VID programming is not required, then the VID section can be disabled by pulling the VIDEN pin low and setting the output voltage with a divider at the output of the differential amplifier. Both phases of the LTC3877 have differential remote sense amplifiers for precise control of the output voltage. The input voltage range of both chips is 4.5V to 38V.

Other features of the LTC3877 include PGOOD pins, RUN pins and TK/SS pins for each rail. The LTC3874 has its own RUN pins and /FAULT pins for quick response to fault conditions.

FPGA Manager IP eases data streaming

Enclustra's FPGA Manager IP solution allows for easy and efficient data transfer between a host and a FPGA over different interface standards



Streaming, made simple.

like USB 3.0, Gigabit Ethernet and PCI-Express. The solution includes a host software library, a suitable IP core for the FPGA and device controller firmware, if necessary. The user host application can communicate with the FPGA through a simple API consisting of simple read/write data commands. Streaming and memory-mapped accesses are supported. The FPGA Manager IP Solution is optimized for Altera and Xilinx FPGAs and greatly simplifies host-to-FPGA communication by hiding the complexity of the underlying protocols. It supports user applications written in C, C++, C# and MATLAB and is available for Microsoft Windows and Linux. When data rates are especially high, PCI Express comes to the fore - FPGA Manager PCIe, with PCIe Gen1 ×4, reaches a bandwidth of over 720 MBytes/s from PC to FPGA, and almost 780 MBytes/s in the opposite direction. Enclustra is continually developing the IP cores to tweak out more performance and adapt them to new technologies — the FPGA Manager IP Solution now supports PCIe Gen2 x4, almost doubling the available bandwidth for host PC to FPGA communication.

Enclustra GmbH
www.enclustra.com

10 favorite FPGA-based prototyping boards

By Adam Taylor

Many FPGA development projects end up as custom-designed boards. During the design and development phase, however, using an off-the-shelf development board facilitates hardware-in-the-loop verification and provides for significant risk mitigation of the more challenging technical aspects associated with getting the system up and running.

We can use these boards for a number of different end applications as such no one board is the magic bullet that enables us to use it for all applications.

Each time we come to select a board for our project we must consider not only the performance of the FPGA or as you will see SoC mounted on it but also the types and size of memories available, the interfaces available, such as USB, EIA232, GigE, among others, along with user-accessible IO allowing integration with elements of the application.

Let us take a look at 10 interesting boards that can be used across a number of different applications.

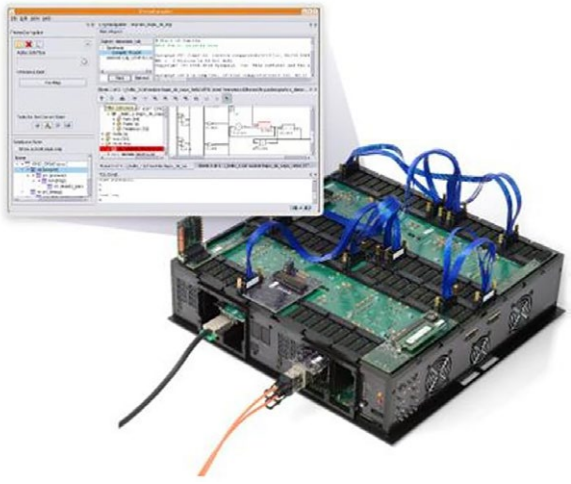
ASIC Prototyping – the High-Performance ASIC Prototyping System (HAPS) board

This is the ultimate development board designed to be used to prototype ASICs across a number of High Performance FPGA's all interconnected within the chassis.

The latest HAPS 80 series comes complete with a Xilinx UltraScale VU440 FPGAs. These high-end devices enable the simulation of up to 1.6 billion ASIC gates on a 64-FPGA HAPS system.

Needless to say a system of this capability requires a significant software suite provided by the ProtoComplier, which configures and controls the prototyping on the system.

This is definitely the high end of development boards, but more than one high-performance signal-processing ASIC currently in orbit was developed using a HAPS system.



HAPS board (Source: www.synopsys.com)

Adam Taylor is a head of engineering systems at E2V -- www.e2v.com

Stratix 5 Development board – high end general development

Moving outside the ASIC prototyping domain, FPGAs themselves are still used in a number of high-performance applications from telecommunications to high-performance RADAR. These applications require development boards that provide high-performance, resource-rich FPGAs but also use high-performance memories such as DDR3, RLDRAM, QDR2+. High-performance IO is also required to move the data on to and off of the system without introducing bottlenecks; therefore this board provides the ability to interface to high-speed mezzanine cards. These can be purchased off the shelf or custom developed for depending upon your application.

This Stratix 5 card from Altera provides all of these along with more common network interfaces like Gigabit Ethernet. Applications include Broadcast, Networking, High Performance Military & Medical systems.

Note, I would have included a Stratix 10 development board but my searches did not find one, if any readers know of any currently available please let me know.

Stratix 5 Development board (Source: www.altera.com)

VCU110 development kit

VCU110 Development Kit (Source: www.xilinx.com)

Another very high end development board based around the Virtex UltraScale device, this board comes with 2 FPGA Mezzanine Card (FMC) slots enabling addition of development specific interfaces along with a wide range of memory type RLDRAM, QDR2+. Most impressively this board is design for high speed networking providing a 28 GBPS backplane interface and both Interlaken and optical interfaces. If your application calls for movement of significant data streams as required in telecommunications or data processing, then this may be the development board for you.

Applications include Broadcast, Networking, High Performance Military & Medical Systems.

MicroZed board

This development board introduced the system on module concept to the FPGA world. It combines a Xilinx Zynq along with DDR, flash, SD card and power management to provide a credit-card sized module that can be integrated into any application or test bench. The MicroZed is a module that you can develop on and then use in your system for the production run.

While this board does not come with many interfaces, the majority of its IO are broken out allowing it to be interfaced to either a specific carrier card like the embedded vision carrier card or the IO carrier card or your own custom developed one.

It also comes complete with a system on chip (SoC) device which combines Dual ARM A9 Cores with FPGA fabric providing true embedded system capability.

Applications for this board include embedded vision, industrial control, security, SDR.

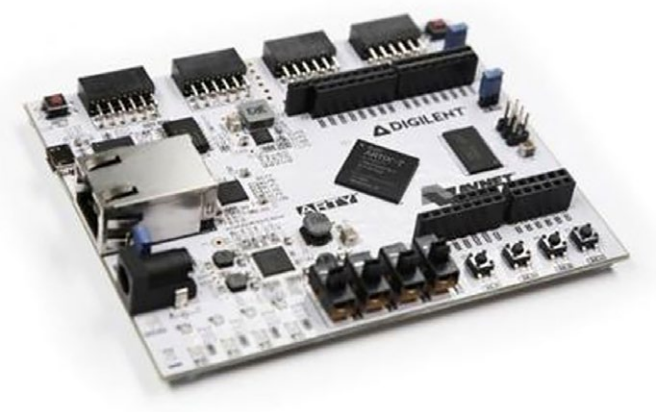
MicroZed Board (Source: http://zedboard.org)

ARTY board

This board is definitely aimed at the lower end of FPGA development but is still very capable. It comes complete with a number of Pmod (peripheral module) interfaces, which provide a common interface standard to a number of peripherals, such as ADC/DAC, H bridges, OLEDs—a rather impressive range of Pmods.

The ARTY board comes complete with an Arduino Shield interface allowing us to develop the FPGA such that we can drive shields or develop our own if the case be.

This board comes with both QSPI flash and DDR3L along with a Vivado Design Suite License. The memory enables us to create MicroBlaze softcore embedded processor applications. The low cost of this board coupled with its capability means that for those simple FPGA projects, you do not need to develop a custom board, just maybe the interface solution.



ARTY Board (Source: www.xilinx.com)

Applications for this board include embedded vision, control applications, SDR, commercial applications.

iCEstick

FPGA design is like any other area of engineering we want to select the right tool for the right job, and there are more FPGA vendors than just Xilinx and Altera. Lattice specializes in the development of small flash-based devices intended for low-power applications—areas which normally preclude the use of a FPGA.

The iCEstick is a simple development board that plugs directly into the USB port on your lap top and provides the FPGA, Pmod interface, IrDa transceiver, and five LEDS.

If your application requires low-power operation modes for instance battery back-up and keep alive functionality, the iCEstick may be just what you need to try out your ideas and de-risk them early in the design cycle.

Applications include battery and low-power applications, system monitoring and security.

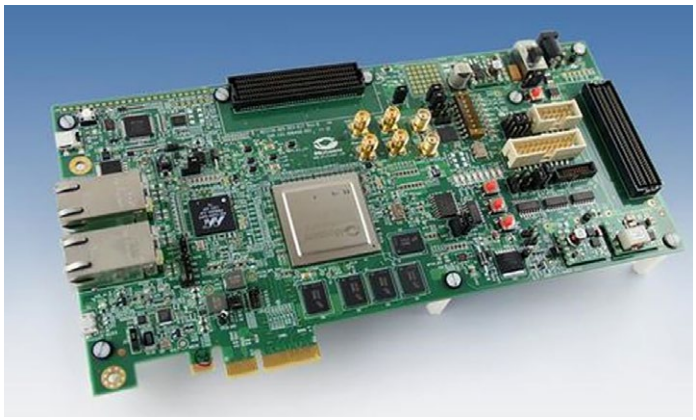
iCEstick (Source: www.latticesemi.com)

Smart Fusion 2 advanced development kit

Sometimes you need to develop a system that is both secure and offers high performance; one of the popular choices for secure systems are flash-based FPGAs as they provide no access to the configuration bit stream.

This development kit, based around the smart fusion 2 SoC, combines FPGA fabric with an embedded ARM Cortex M3 processor. The development board comes with a wide range of memory technologies and FMC (FPGA Mezzanine Card) interfaces.

Typical applications for development board may be industrial, power or military applications.



Smart Fusion 2 advanced development kit (Source: www.microsemi.com)

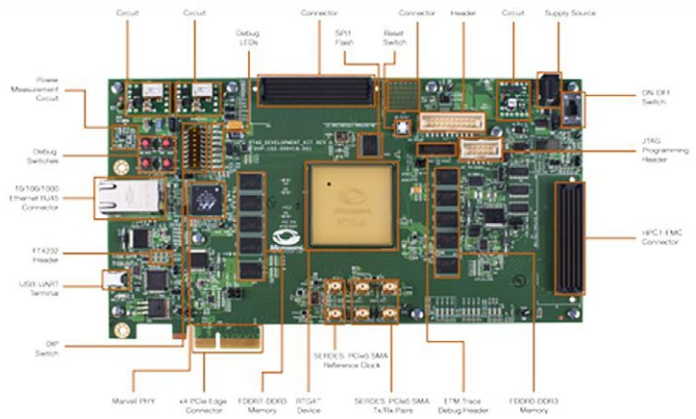
RTG4

They say in space no one can hear you scream, and if you are developing a FPGA for a space application, using this development board will stop you from screaming.

Microsemi's RTG4 board features the new Radiation Tolerant Pro ASIC 4 FPGA, which was developed for demanding space applications, and comes with a very capable logic fabric, SERDES interfaces and specialized SpaceWire clock recovery circuits.

The board itself features all of the necessary interfaces to enable hardware in the loop testing such as PCIe, GigaBit Ethernet interfaces and of course FMC interfaces allowing you to connect to representative circuits of your final hardware design.

Applications for this board include developing satellite communication processors, mass memory controllers, and payload controllers.



RTG4 (Source: www.microsemi.com)

Parallella board

The Parallella Board is a very interesting board that combines a Xilinx Zynq FPGA along with the Epiphany 16 core co-processor. This combo makes the credit-card sized board capable of high performance while being power efficient. The Epiphany co-processor is connected to the Zynq, which acts as the master, where applications are concerned. There is also the FPGA logic side of the Zynq that can be programmed to make the performance even better.

This board also has a number of IO available on the bottom making it able to be mounted as a system on module like the MicroZed as well as coming with the usual Gigabit Ethernet and HDMI output interfaces.

Coupled with the new SDSoC tool from Xilinx, which allows you to partition easily between hardware and software, the Parallella board can prove very capable.

Typical applications include control, instrumentation, SDR.

The Parallella board (Source: www.parallella.org)

Arria SoC

One of the newest SoC development kits from Altera, the Arria SoC device combines dual-core ARM A9 processors with flexible FPGA programmable logic.

The Arria SoC development board comes packed with IO Standards from FMC (which is a welcome change from the previous HSMC connectors) to Gigabit Ethernet, plus DDR, SD card slot and QSPI to get your designs up and running.

This device is very similar to the Xilinx Zynq and has many of the same applications such as embedded vision, industrial control, security, SDR, defense applications.

High, mid, or low

I have briefly introduced a number of different FPGA development boards from a range of vendors, which hopefully provides some understanding of the available boards and the devices. Of course, the range of FPGA development boards is wide and choice increases daily.

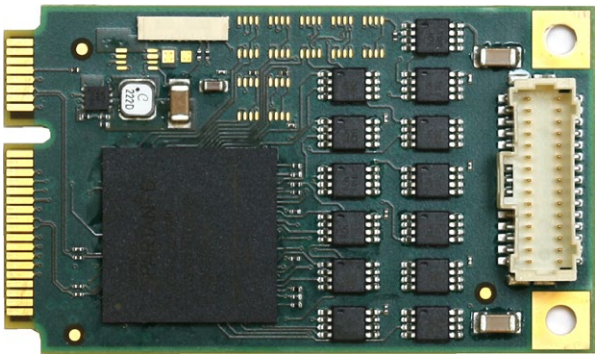
What is important is understanding your project requirements for your application do you really need a high-end development board or will something mid-range do.

Depending upon the number of units you are intending to produce, many of these development boards could form the core of your implementation. After all, as engineers we should be focusing upon where we can best add value to the design process.

Arria SoC (Source: www.altera.com)

mPCIe modules host user-programmable FPGA

Tews Technologies (Halstenbek, Germany) has designed a standard full PCI Express Mini Card with a user programmable Xilinx Spartan-6 LX25T FPGA. The TMPE633 is designed for industrial, COTS, and transportation applications, where specialized I/O or long-term availability is required. It provides a number of advantages including a customizable interface for unique customer applications and a FPGA-based design for long-term product lifecycle management. TMPE633 module versions are available with either 26 ESD-protected 5V-tolerant TTL lines, 13 differential I/O lines with EIA 422/485 compatible ESD-protected line transceivers or 13 differential I/O lines using Multipoint-LVDS transceivers. All I/O lines are individually programmable as input or output. TTL I/O lines can be set to high, low, or tristate. Each TTL I/O line has a pull-resistor to a common programmable pull-up voltage that can be set to +3.3V, +5V and GND. Differential I/O lines are terminated, RS-485 lines with 120Ω and M-LVDS lines with 100Ω. The I/O signals are accessible through a 30 pin Pico-Clasp latching connector. The User FPGA is configured by a SPI flash. An in-circuit debugging option is available via a JTAG header for read back and real-time debugging of the FPGA design (using Xilinx "ChipScope"). With TEWS' TA308 Programming Kit, direct JTAG access to the FPGA is possible using the Xilinx Platform Cable USB. User applications for the TMPE633 with XC6SLX25T-2 FPGA can be developed using the design software ISE WebPACK which can be downloaded free of charge from www.xilinx.com TEWS offers a documented basic FPGA Example Application design. It includes an .ucf file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TMPE633. It implements local bus interface to local bridge device, register mapping and basic I/O. It comes as a Xilinx ISE project with source code and as a ready-to-download bit stream. In order to support long term programs, the TEWS' modules have a 5 year warranty.

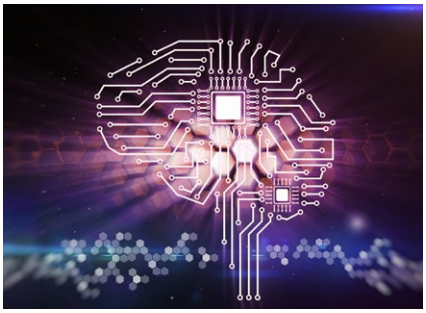


Tews Technologies
www.tews.com

Embedded neural networks: Cadence's latest DSP target

With up to four times the neural network performance capability of Cadence's previous-generation vision DSP, the Tensilica Vision P6 DSP is the company's highest-performing vision/imaging processor. The new IP extends the Tensilica product portfolio further into the fast-growing vision/deep learning applications areas. It quadruples multiply-accumulate (MAC) performance compared to the previous generation Vision P5 DSP, targeting convolutional neural network (CNN) applications which are dominated by available MAC performance. Compared to commercially available GPUs, the Tensilica Vision P6 DSP can achieve twice the frame rate at much lower power consumption on a typical neural network implementation, claims the company. For a wide range of other key vision functions, such as convolution, FIR filters and matrix multiplication, the Tensilica Vision P6 DSP increases performance by up to 4X by utilizing its improved 8-bit and 16-bit arithmetic. In addition, the new IP implements on-the-fly data compression to sharply reduce memory footprint and bandwidth requirements for demanding "fully connected" neural network layers.

Compatible with the Vision P5 DSP, this newest vision DSP offers an optional 32-way SIMD vector floating-point unit that includes the IEEE half precision standard (FP16). Floating-point performance capability is double that of the Vision P5 DSP, enabling easy use of existing floating-point neural network implementations. "Cadence is investing heavily on advanced vision and deep learning," said Chris Rowen, CTO for the IP Group at Cadence. "We are devoting intense efforts to discovering improved structures and training for neural networks, providing rich software environments for fast application development and offering breakthrough vision DSP architectures for embedded vision and learning deployment. The Tensilica Vision P6 design is the direct result of this investment and significantly raises the bar in both vision efficiency and scalability." The Tensilica Vision P6 DSP is based on the Cadence Tensilica Xtensa architecture, and combines flexible hardware choices with a library of vision/imaging DSP functions and numerous vision/imaging applications from our established ecosystem partners. It also shares the comprehensive Tensilica partner ecosystem for other applications software, emulation and probes, silicon and services and much more.



Cadence
www.cadence.com

Diamond ICs may finally debut

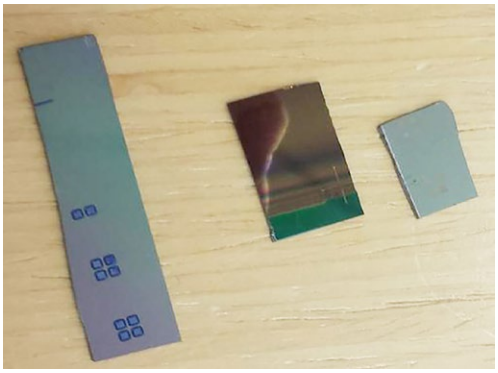
By R. Colin Johnson

Diamonds may soon be the semiconductor industry's "best friend." Startup Akhan Semiconductor Inc. (Gurnee, Ill.) plans to make the promise of diamonds come true by licensing the diamond semiconductor process from the U.S. Energy Department's Argonne National Laboratory (Lemont, Ill.).

Diamond semiconductors have been known to be faster, consume less power, be thinner and lighter weight that silicon, but Akhan Semiconductor is the first vendor with its foot-in-the-door of actually realizing its capabilities.

Akhan Semiconductor has a 200mm wafer fab in Gurnee, Ill. and expects to announce a diamond semiconductor IC in a consumer product at the Consumer Electronics Shows (CES) 2017.

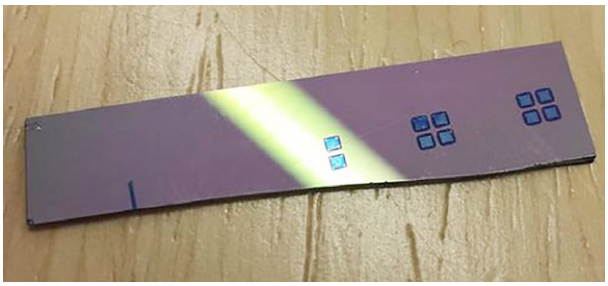
Since before 2000, Argonne National Lab has been experimenting with diamond chemical vapour deposition (CVD), spinning off Advanced Diamond Technologies Inc. who partnered with Innovative Micro Technology to produce diamond micro-electromechanical systems (MEMS) and inspiring diamond wafer specialists like SP3 Diamond Technologies (Santa Clara, Calif.) to create the CVD equipment to deposit perfect crystalline diamond.



Samples of diamond on silicon from Akhan Semiconductor. Adam Khan, CEO of Akhan, showed samples to EE Times on May 3rd, 2016. (Source: EE Times)

So far, however, the biggest successes for diamond have been in jewelry, abrasives and other industrial uses of man-made diamonds. Nevertheless, Argonne National Labs continued pursuing the dream of diamond semiconductors by finding a way to make diamond—a natural insulator—into a semiconductor and a conductor laying out the path to all diamond chips.

The biggest problem that kept diamond from being commercialized, until now, has been the ease of making p-type transistors, but the difficulty of making n-types, a problem solved by founder and chief executive officer of Akhan Semiconductor, Adam Kahn, who dubbed his process the Miraj Diamond Platform. With both p- and n-type devices, diamond complementary metal oxide semiconductors (CMOS) are now possible. And Akhan Semiconductor hopes to roll out the world's first CMOS-compatible diamond semiconductors.



Sample of diamond on silicon from Akhan Semiconductor, May 3, 2016. (Source: EE Times)

"We recently demonstrated CMOS-compatible diamond semiconductors—with both p-type and n-type devices—by successfully fabricating diamond PIN [abbreviation for a p-type—intrinsic, undoped—n-type junction] diodes with a million-times better performance than silicon and one-thousand-times thinner," Khan told EE Times in an exclusive interview.

Its secret was co-implanting phosphorous in p-type devices and co-doping borium and lithium into n-type devices, resulting in tuneable electronics that achieve comparable performance in both types, thus enabling diamond CMOS. The company's first demonstrated device, however, was a diamond PIN diode that was a record-breaking 500 nanometers thin. This type of performance is due to diamond being a super wide band-gap material—wider than even silicon carbide and gallium nitride.

"Thermal analysis showed that there were no hot spots on our PIN either, so there were no parasitic losses like with silicon PIN diodes," Khan told EE Times.

Khan has also demonstrated 100-Giga-Hertz (GHz) devices by virtue of the ultra-low resistance of diamond, which can be deposited on silicon, glass, sapphire or metal substrates. Those kind of speeds could revitalize the processor races, which have been idled at 5-Ghz for a decade. Remember when every new processor was clocked at a higher rate. With silicon, 5-GHz is the limit, since their high power consumption and thermal hot-spots turn devices into soup, but diamond has 22-times the thermal conductivity of silicon and five-times that of copper, Kahn claims.

The company's ultimate goal is to revitalize the processor race with faster and faster clock rates, but for now they are concentrating on power electronics for industry, tuneable optical military applications for countermeasures, and optical mobile consumer applications using diamond as the insulator and semiconductor, but still requiring indium tin oxide (ITO) for contacts (for now).

After banking some successful applications for angel investors and private equity firms who have provided Akahn's research and development capital so far (to the tune of about $2.5 million). Akahn plans to announce Series A funding later this year, prompting them to come out of the closet at this time to attract a little attention about the possibilities that diamond semiconductors hold.

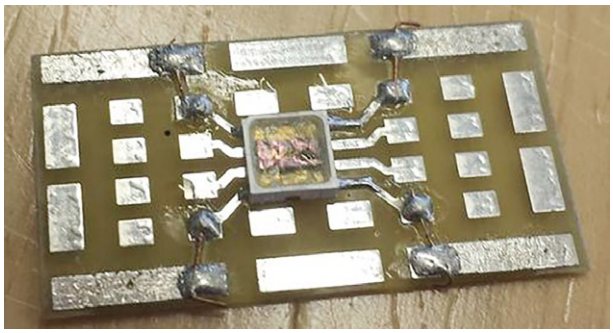
"We are not developing our mobile and consumer platform yet. For now our major application is power electronics that is more heat efficiency, but which works just like silicon devices—using the same lithograph, etching and metallization steps—just adding the diamond deposition step," Kahn told us.

But its ultimate goal is to take-the-heat-off (literally) of Big Data applications with ultra-cool-running processors.

In fact, the high speeds capable of diamond CMOS is traded off against heat. In other words, data centres could cut their heat vastly, by running diamond processor at the same 5-GHz of silicon, or could bump up their speed to the sub-terahertz range while consuming the same power as silicon.

"Heat is our major issue—half of big data energy today is wasted just keeping its silicon processors cool," Kahn told us. "Diamond is the next obvious step because it is much more energy efficient. It can also be deposited on glass and sapphire to make completely transparent electronics—for consumer applications, such as transparent mobile devices."

Moore's Law will also be extended—yet again—according to



Sample board with diamond heat sinks (a chip can sit directly on top of a heat sink). Adam Khan, CEO of Akhan Semiconductor, showed the sample to EE Times on May 3, 2016. (Source: EE Times)

Kahn, since the 100-GHz demonstration chips it is showing now use design rules in the 100s of nanometres. That leaves almost a dozen generations of shrinkage before diamond faces the single-atom levels the silicon is facing circus 2025.

"Today we are focusing on power applications on 12-inch wafers, hoping to drive down the costs of production with higher volumes," Kahn told us. "Our power devices are moving into pilot production at our own fab, but we are using the fab-lite model—that is produce small- to medium-sized runs ourselves, then transferring our process to foundries when we ramp up into volume production."

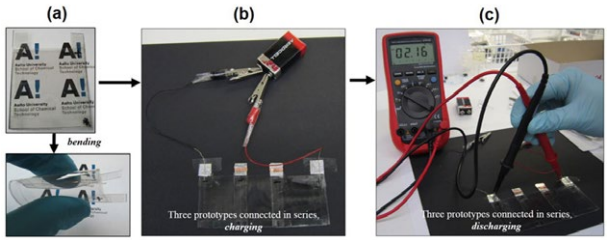
Besides power devices, Akahn also claims to have fledgling customers for diamond MEMS devices—specifically for capacitive switching arrays used to dynamically tune antenna in high-end smartphones.

Next, besides mobile and data-center processors, Akahn aims to enter the quantum computer field, but not using the nitrogen vacancy method, but rather using their own proprietary doping techniques they are keeping as a trade secret for now.

Transparent supercapacitors soon integrated into displays?

By Julien Happich

Researchers from Aalto University (Finlande) and the Skolkovo Institute of Science and Technology (Russia) have demonstrated a fully transparent electrochemical double-layer capacitor relying on single-walled carbon nanotube (SWCNT) films for their electrodes.



Photos of a transparent and flexible EDLC prototype based on the thin SWCNT films. (b) Charging and (c) discharging of three EDLC prototypes connected in series. Credit: Kanninen et al. ©2016 IOP Publishing

The SWCNT films obtained exhibited extremely large specific capacitance (178F g^{-1} or 552μF cm^{-2}), high optical transparency (92%) and stability for 10 000 charge/discharge cycles, the scientists report in their paper "Transparent and flexible high-performance supercapacitors based on single-walled carbon nanotube films". These properties make the SWCNT films well suited to design flexible and high-performance transparent and flexible energy storage devices to be used in displays, sensors or photovoltaic applications, to name a few.

The researchers devised a single step aerosol synthesis and dry deposition method to produce the SWCNT thin films which were used as electrodes for an electrochemical double-layer capacitor (EDLC) prototype constructed with a polyethylene casing and a gel electrolyte.

Lead author Petri Kanninen sees potential applications for high-aesthetic-value products, such as activity bands and smart clothes, and inherently transparent end-uses, such as displays and smart windows.

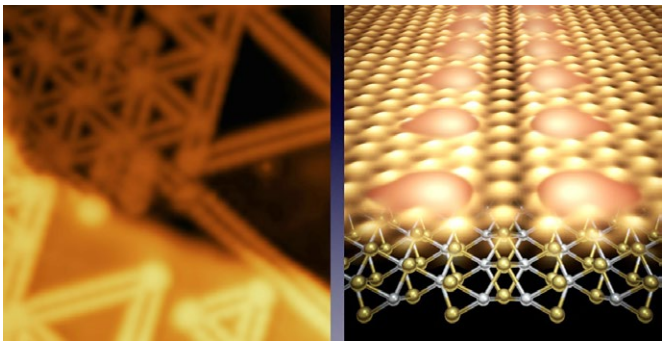
The researchers are now working on a stretchable version of their SWCNT-based supercapacitor, hoping to reach up to 100% elongation without loss of performance.

Exploring linear defects in 2D semiconductors

By Julien Happich

In a recent paper published in Nature Physics, "Charge density wave order in 1D mirror twin boundaries of single-layer $MoSe_2$", scientists from the Department of Energy's Lawrence Berkeley National Laboratory (Berkeley Lab) and UC Berkeley highlight how linear defects in 3-atom thin layers of molybdenum diselenide affect the material's electronic behaviour.

Under the scrutiny of a modified scanning tunnelling microscope, which the scientists "sharpened" by placing a single carbon monoxide molecule at the very end of the probing tip, the $MoSe_2$ 2D material revealed linear defects formed by lines of missing selenium atoms, creating one-atom thick metallic wires. Also described as 1D mirror twin boundaries across the 2D semiconductor sheets, the defects when cooled down to -269ºC (about 4ºK) caused the atoms along the metallic wires to rearrange themselves, giving place to a charge density wave (the atoms' electrons no longer being uniformly distributed, but instead, modulated like a sinusoidal wave along the metallic wires).



The left microscopy image shows linear defects that cross the 2-D semiconductor like veins. The defects are located between the parallel lines. The right image is a combination of the theoretical atomic structure on the bottom, and a microscopy image on top that shows individual selenium atoms in gold and the charge density wave in red. (Credit: Berkeley Lab)

According to the researchers, the presence of a charge density wave is especially intriguing because it indicates a strong coupling between the electrons, mediated by the atomic lattice, noting that similar strong coupling happens in superconducting states.

Although they used liquid nitrogen to reach the 4ºK temperature of their experiments, the charge density wave was still observable at higher temperatures, which pushes the researchers to investigate other types of Transition Metal Dichalcogenides (TMDs) in search of new high temperature superconductors.

The research was conducted by Alexander Weber-Bargioni, D. Frank Ogletree, Sara Barja, Sebastian Wickenburg, Zhen-Fei Liu, and Jeff Neaton of Berkeley Lab's Molecular Foundry. In addition, scientists from Berkeley Lab's Advanced Light Source and Materials Sciences Division contributed to the research.

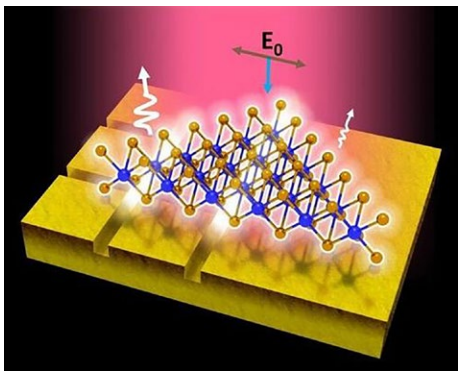
Breakthrough boosts 2D semiconductor photoluminescence

EE Times Asia

Researchers from the National University of Singapore (NUS) have come up with a technique to enhance the photoluminescence efficiency of tungsten diselenide, a 2D semiconductor. According to them, the discovery could light the path for the application of such semiconductors in advanced optoelectronic and photonic devices.

Tungsten diselenide is a single-molecule-thick semiconductor that is part of an emerging class of materials called transition metal dichalcogenides (TMDCs), which have the ability to convert light to electricity and vice versa, making them strong potential candidates for optoelectronic devices such as thin film solar cells, photodetectors flexible logic circuits and sensors. However, its atomically thin structure reduces its absorption and photoluminescence properties, thereby limiting its practical applications.

By incorporating monolayers of tungsten diselenide onto gold substrates with nano-sized trenches, the research team, led by professor Andrew Wee of the department of physics at the NUS Faculty of Science, successfully enhanced the nanomaterial's photoluminescence by up to 20,000-fold. This technological breakthrough creates new opportunities of applying tungsten diselenide as a novel semiconductor material for advanced applications.



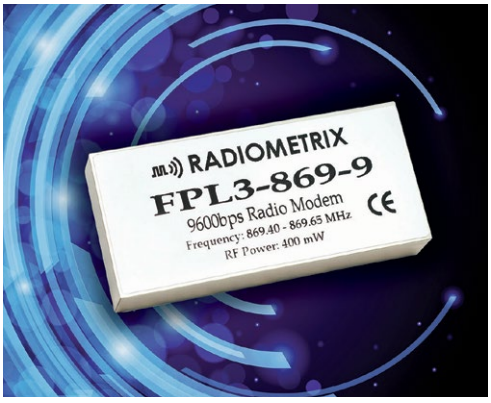
This is a schematic of the light emission from a single crystal monolayer of tungsten diselenide flake on a gold substrate. Part of the triangular flake rests on the patterned region of the substrate consisting of sub-20nm wide trenches. (Source: NSU)

Wang Zhuo, a PhD candidate from the NUS Graduate School for Integrative Sciences and Engineering (NGS) and first author of the paper, explained, "This is the first work to demonstrate the use of gold plasmonic nanostructures to improve the photoluminescence of tungsten diselenide, and we have managed to achieve an unprecedented enhancement of the light absorption and emission efficiency of this nanomaterial."

Elaborating on the significance of the novel method, Wee said, "The key to this work is the design of the gold plasmonic nanoarray templates. In our system, the resonances can be tuned to be matched with the pump laser wavelength by varying the pitch of the structures. This is critical for plasmon coupling with light to achieve optimal field confinement." Moving forward, the research team will further investigate the effectiveness of the lateral gold plasmon in enhancing the second harmonic generation and electroluminescence of TMDCs.

400mW radio modem for long range telemetry in Europe

The Radiometrix FPL3 radio modem simplifies the design of long range wireless appliances that can be marketed in any European country. This highly integrated multi-channel radio with 400mW RF output power operates in the 869.4-869.65 MHz frequency band, which is the only band permitted for license-free operation at up to 500 mW in all EU countries. The FPL3's built-in modem minimises demand for external components. The modem has inverted-RS232 serial interfaces at 5V CMOS voltage level, which enables direct connection to a UART or host microcontroller without a driver or level shifter. The FPL3 also integrates firmware for managing data timing and formatting at the radio interface, which saves the user keying the transmitter on or off and ensures dependable link latency. With maximum serial data rate of 9600 baud and radio range of more than 3 km, depending on operating conditions, the FPL3 can be used in security systems, fire-warning systems, industrial controls or telemetry, asset tracking, and control of remotely operated vehicles (ROVs). The eight-channel radio is programmed for 869.475MHz and 869.565 MHz in the EU, with channels 4-7 set to 869.50 MHz for backward compatibility. The 67x30x12mm module operates from a single 5V supply, and draws 50mA in receive mode and 500mA when transmitting at 400mW (+26dBm) RF output power. The FPL3 conforms to ETSI EN 300 220-2 (radio) and EN 301 489-3 (EMC) standards.



Radiometrix
www.radiometrix.com

Parallax-free IR and visible imaging under one lens

Researchers at the Fraunhofer Institute for Photonic Microsystems (IPMS) in Dresden have developed a high-resolution camera which produces images combining two spectral ranges using multiple detectors through a single lens.

While systems currently available on the market use costly optics, materials and components individually adapted for various spectral ranges, the multi-spectral camera invented by Fraunhofer IPMS uses two image sensors behind a common lens designed as a special tilted mirror system. By construction, the lens avoids the chromatic aberrations or central obscuration effects occurring in competing systems. Individual mirror surfaces have been designed in a partially aspheric manner to correct geometric aberrations and are provided with suitable coatings to ensure high reflectivity over a wide spectral range.

Because the camera captures information in different spectral ranges through a single lens, it delivers simultaneous parallax-free images that are simpler to process (no parallax corrections and overlay matching).

The choice of the spectral range of the reflective optics is then limited only by the detectors available. Fraunhofer IPMS researchers have now integrated the lens and image sensors with electronics and software in a first functional demonstrator.

Fraunhofer IPMS
www.ipms.fraunhofer.de

LED-based lightguides target wearables

Addressing both the requirements of functional illumination (backlighting and front-lighting of displays and indicators) and decorative illumination (contours, logos), Global Lighting Technologies (Brecksville, OH) puts its thin lightguide technology to the fore. For wrist-worn devices, GLT produces lightguides as thin as 0.25 mm, using as few as one LED to illuminate LCDs in conventional, GPS, and fitness watches. This not only allows for a thinner profile on the user's wrist, but also enables a decrease in power consumption, resulting in increased battery life and enhanced performance. With proper design and LED coupling, the efficiency and uniformity of these backlights can outperform much thicker lightguides, the company claims. In the clothing side of the wearables market (including accessories), GLT has products in the 0.25 mm to 0.40 mm thickness range made of polycarbonate (PC) material that can be flexible. These lightguides can be combined with single colour LEDs as well as RGB (red, green, blue) LEDs to produce backlights for logos and decorative elements. For the head-worn market including AR and VR devices, GLT has created customized lightguides with focused and directed light emissions patterns necessary for the proper illumination of displays. This assists with the performance by directing the projection of images from the LCD to the eye creating the final user experience.

Global Lighting Technologies
www.glthome.com

Piezo nanopositioning stages offer 0.02nm resolution

Aerotech's QNPHD linear piezo nanopositioning stages provide the benefits of both a stage and actuator in one compact, high-stiffness package. With a direct-metrology, capacitive sensor feedback option, high resonant frequencies up 6300Hz and high load capacity, the QNPHD is well suited for a wide range of high-speed and high-precision applications such as scanning probe microscopy, disc-drive testing, and semiconductor wafer articulation. A direct-drive actuation design and optimized structure enable millisecond response and move-and-settle times. FEA optimized precision flexures ensure high-stiffness, long device life, and high-dynamics while maintaining excellent geometric performance (straightness and angular errors) for critical nanopositioning applications. Optional closed-loop feedback using a unique capacitive sensor design allows for 0.02nm resolution and 0.02% linearity errors. The capacitive sensors measure the output of the positioning carriage directly enabling superior accuracy and repeatability. The QNPHD is available with rear and side cable exit options along with mounting features for both horizontal and vertical orientations.

Aerotech
www.aerotech.com

Home automation gets dedicated cryptographic code and core

Oberon microsystems and Cortus have joined their forces to secure home automation, porting and optimizing Oberon's cryptographic code to the Cortus APS3RP 32-bit IP core. The combination of the tiny software memory footprint and minimalist processor core is well suited to secure ASICs in battery-powered home automation devices. Oberon microsystems has developed, analysed and optimised the cryptographic code of OberonHAP since 2013. The company has developed and formally proved novel algorithm combinations, and has carefully written critical parts in assembly language for high performance. The resulting software is typically three times as fast as a good implementation in C, enabling secure home automation even on low-power, low-cost 32-bit microcontroller cores for ASICs. For pairing, authentication and encryption, OberonHAP implements Secure Remote Password (SRP), Ed25519, Curve25519, HKDF-SHA-512 and ChaCha20-Poly1305. For an integrated circuit with the processor core running at 50 MHz, the cryptographic processing of the SRP algorithm – which is required once in the lifetime of a home automation device – takes less than five seconds. Cryptographic processing during opening of a session between a device and a smartphone takes less than 100 milliseconds. RAM requirements were brought down to a record-low 2.5 KB. The APS3RP is an enhanced performance version of the widely-deployed APS3R and provides a single cycle parallel multiplier.

Cortus S.A.S.
www.cortus.com

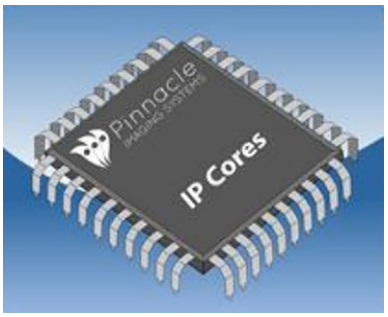
Ultra low jitter high frequency SAW oscillator

The VS-708 is a Voltage Controlled SAW Oscillator (VCSO) that operates at the fundamental or a fraction of the internal SAW lter frequency and is the latest addition to the Vectron's VCSO ultra low jitter oscillator family. Packaged in an industry standard 5.0x7.5mm footprint, this VCSO offers a jitter performance of 55 fs-rms over the offset bandwidth of 12 kHz to 20 MHz, with a frequency range of 600 MHz to 2.3 GHz. This product is ideal for emerging optical transport networks and supporting high speed ADCs that demand a low jitter high frequency reference clock. Other features of the VS-708 include absolute pull range ±50ppm; LVPECL or LVDS compatible outputs (fN < 1.2 GHz); and differential sinewave compatible outputs (fN > 1.2 GHz). The device supports 3.3 V operation in a 5.0x7.5x2.0mm package. The SAW component is a high-Q Quartz device that enables the circuit to achieve low phase jitter performance over a wide operating temperature range. The oscillator is housed in a hermetically sealed leadless surface mount package and offered on tape and reel. It has a tri-state Output Enable function that provides one of three conditions: Outputs Enabled, Outputs Set, or Outputs Disabled.

Vectron
www.vectron.com

Pinnacle Imaging offers library of imaging cores

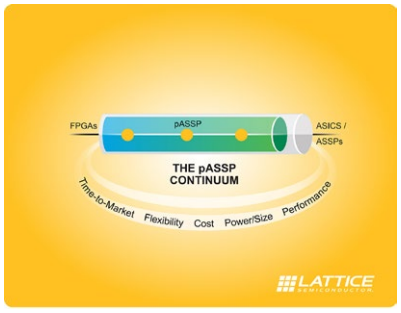
Pinnacle Imaging Systems Corp. (Belmont, Calif.) has developed and begun licensing its Ultra HDR family of cores for use in high dynamic range (HDR) video and still cameras. Pinnacle has a track record in providing software for maximizing dynamic range in captured images and has now ported that expertise into a library of IP cores that covers such activities as frame merging and locally adaptive tone mapping (LATM). The IP cores sit between – and work independently of – the image sensor and the downstream logic. The company cites the example that some sensors produce up to 115dB of dynamic range non-natively, at 1080p/60fps, and may not need further dynamic range improvement for the application, but could benefit from LATM IP cores for adaptive scene improvement for each frame. Similarly, some sensors produce about 65dB of dynamic range in their native mode and can utilize an added boost in range to 120dB by use of a four- or two-frame merge with no visible artifacts for improved motion capture. Applications that can benefit from the enhanced dynamic range to counteract high brightness, glare and deep shadow include security and surveillance, intelligent traffic and transportation systems, after-market automotive camera systems, wearable camera and vision systems. Other cores can provide automatic ghost removal and halo reduction and compensate for minimal camera motion between frames, automatic white balance and exposure controls, and shadow tracking tracking. The architecture of the IP cores is modelled in human vision and seeks to preserve a scene's true colors during the tone mapping process. The Ultra HDR technology can capture 120 fps (merging four exposures per frame), and stream full 1080 HDMI tone mapped video for display at up to 60 fps in real time. "We are currently seeing growing demand for HDR capabilities embedded into video cameras and production equipment," said Ron Tussy, director of business development for Pinnacle Imaging Systems, in a statement. "Our proprietary embedded HDR tone mapping is a critical underlying technology necessary to improve data capture for technologies used in range finding and recognition in automotive, security and surveillance or any other field demanding video to be captured across very bright and very dark areas." Initial FPGA implementations have been completed and the Ultra HDR IP blocks can now be ported to silicon implementations within ASICs, DSP+SoCs or ISPs. Development kits are also available.



Pinnacle Imaging Systems
www.pinnacleimagingsystems.com

Programmable ASSP interface bridge for mobile image sensors and displays

Lattice Semiconductor has applied its medium-scale programmable logic to a variety of bridging and signal conversion tasks; now it is combining it with 'hard' (diffused fixed-function) blocks to create a series of chips that are dedicated to specific signal types, but retain the flexibility of the programmable logic element. The company's CrossLink is a low cost video interface bridge claiming highest bandwidth, lowest power and smallest footprint; is is conceived to resolve interface mismatches between mobile application processors, image sensors and displays. Applications envisaged include VR, drones, cameras, wearable devices, mobile devices and human machine interfaces (HMIs). The architecture is that of dedicated physical interfaces (transceivers) at the I/O ports of the chip, with a block of OTP (one-time-programmable) FPGA in the centre. You program the FPGA (create the configuration code) in Lattice's Diamond software; Lattice supplies appropriate functions as importable IP; this IP is provided in source form and is compiled in the Diamond environment, and is there open to customisation. The FPGA 'core' usage for typical applications amounts, Lattice has found, to around 2700 to 4300 LUTs. Lattice adds that its highest-growth area is automotive, and the devices are designs to be AECQ 100-qualified, a step which will follow at a later time. Systems with embedded cameras and displays often, Lattice asserts, do not have the right type or number of interfaces, which can be resolved using a bridge. The CrossLink device combines the flexibility and fast time to market of an FPGA with the power and functional optimization of an ASSP to create a new product class the company calls programmable ASSP (pASSP).



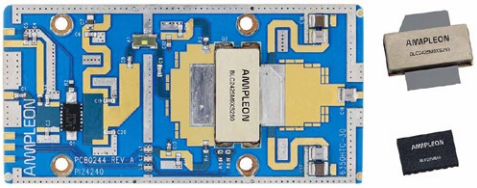
The CrossLink device's features include:
- Fastest MIPI D-PHY bridging device that delivers up to 4K UHD resolution at 12 Gbps bandwidth.
- Supports popular mobile, camera, display and legacy interfaces such as MIPI D-PHY,
MIPI CSI-2, MIPI DSI, MIPI DPI, CMOS, and SubLVDS, LVDS and others.
- Smallest package size with a 6 mm ^{2} option.
- Lowest power programmable bridging solution in active mode.
- Built-in sleep mode.

CrossLink can multiplex, merge and arbitrate between multiple image sensors to a single input. The device can also interface between high-end industrial and popular A/V image sensors with mobile application processors. This is suitable for 360, action, surveillance and DSLR cameras along with drones, and augmented reality products.With the CrossLink device, it is possible to receive video data from one MIPI DSI interface and send it out over two MIPI DSI interfaces at half the bandwidth. The same video stream can be split to two interfaces, for virtual reality headsets and mobile set top boxes. Designers can also integrate consumer and industrial panels with RGB or LVDS interfaces with mobile applications processors. The CrossLink bridge can convert from MIPI DSI to multiple lanes of CMOS or LVDS interfaces such as MIPI DPI, OpenLDI and proprietary interface formats for HMIs, smart displays, and smart homes. CrossLink evaluation boards are available from Lattice and its distributors and production devices will be available shortly

Lattice Semiconductor
www.latticesemi.com/CrossLink

Reference design for solid-state RF cooking

Ampleon has released a 250-W, 2.4 to 2.5 GHz amplifier reference design, the MicroBlaze 250, measuring just 80x40x5mm and designed for use in RF cooking and industrial heating designs where power controllability and a modular design approach are key criteria.



The LDMOS-based MicroBlaze 250 is fabricated on a copper base plate using cost optimized PCB materials and uses Ampleon's BLC2425M9XS250 ACP-3 air cavity package and BLP27M810 power transistors. It is fully balanced in terms of gain and power efficiency and is a ready-to-copy amplifier reference design that can be incorporated into an end product. Full optimized for BOM cost, customers can gain a significant time-to-market advantage by using this reference design in their application. With a 21 dBm input the MicroBlaze 250 provides a 36 dB gain and a 250 W output measured at P1dB compression. The module has a rugged VSWR characteristic and can sustain 60 seconds up to 10:1. It is powered from a + 32 VDC supply and consumes 20 A. Capable of operating in most environments it has an operating temperature range of + 5 to + 100°C.

Ampleon
www.ampleon.com

High frequency RF SOI mixer covers 10 to 19 GHz

Peregrine Semiconductor has added the UltraCMOS® PE41901 high frequency image reject mixer into its growing portfolio of high frequency RF SOI products. This complete MMIC is based on the company's UltraCMOS technology and provides reliable, repeatable and consistent frequency-mixing. Image reject mixers provide an integrated phase-canceling capability by removing the unwanted image signal from the output. This type of mixer reduces the number and complexity of the filters required in a system, resulting in minimized board space and design effort.

The PE41901 is the company's first image reject mixer and its first mixer at high frequencies. The UltraCMOS PE41901 is a passive double-balanced, Ku band mixer with image rejection. It integrates two mixers, a local oscillator (LO) path 90-degree coupler and RF port baluns on a single die. Integrating these functions provides good image rejection, reduces LO leakage and improves LO to RF isolation.

This mixer operates with single-ended signals on the RF and LO ports, and it can be used as an upconversion or downconversion mixer. It supports a broad RF frequency range of 10 to 19 GHz. The intermediate frequency (IF) port accepts broadband quadrature signals from DC to 4 GHz, while the LO port covers a frequency range of 12 to 19 GHz.

Peregrine Semiconductor
www.psemi.com

Three PC-based oscilloscopes to take away

This month, Pico Technology is giving away three PicoScope 2208B 100MHz Mixed Signal deep-memory Oscilloscopes (MSO), worth 859 Euros each, for *EETimes Europe*'s readers to win.

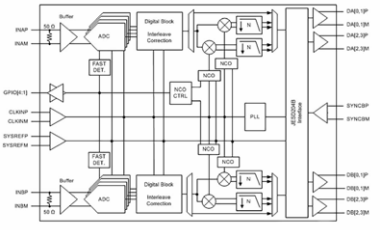
Combining four instruments in one with two analog channels and 16 digital channels, the compact unit features an FFT spectrum analyzer, a function generator, an arbitrary waveform generator and a protocol decoder with support for 15 serial protocols. The PicoScope 2000B models come with up to 128MS of deep memory and fast waveform update rates to carry out advanced analysis of waveforms, including serial decoding and plotting frequency against time.

The instrument comes with the PicoScope 6 software, taking advantage of the display size and resolution and processing power of your PC to display four analog signals, a zoomed view of two of the signals (undergoing serial decoding), and a spectrum view of a third, all at the same time. Unlike a conventional benchtop oscilloscope, the size of the display is limited only by the size of your computer monitor. The software is also easy to use on touch-screen devices, so you can pinch to zoom and drag to scroll.

Check the reader offer online at
www.electronics-eetimes.com

Gigahertz 14-bit ADC eases direct conversion RFx

Texas Instruments has introduced a 14-bit analog-to-digital converter (ADC) that runs at up to 3-gigasamples per second and priced at $2,495.00 This dual-channel ADC, the ADC32RF45 enables direct RF signal conversion up to 4GHz and can eliminate up to four intermediate-frequency down-conversion stages in multiband receivers if users shift to direct down conversion. Direct RF sampling meets engineers' requirements for higher integration, better noise performance, wider bandwidth and smaller footprints in radar, software-defined radio, aerospace and defense, test and measurement, wireless communication, and radio astronomy systems. The ADC32RF45 offers a signal-to-noise ratio of 58.5 dB at a 1.8-GHz input frequency. TI is offering an evaluation module for the part, the ADC32RF45EVM, priced at $2,499.00. The ADC32RF45 will be in volume production in the third quarter of 2016 in a 72-pin, 10mm by 10mm quad flat no-lead (QFN) package for US$2,495 in 100-unit quantities.



Texas Instruments
www.ti.com

Multifunction waveform generator spans simple AFG to complex sequences

Tektronix describes its AWG4000 Series as a 3-in-1 arbitrary waveform generator; with basic, advanced and digital modes, the portable signal generator can be shared across design teams and can meet a wide variety of signal generation needs ranging from radar and wireless communications to embedded systems design and research applications. AWG outputs may be as simple as a clock with constant frequency in an embedded design, or as complex as a mix of modulated waveforms in parallel with digital patterns in radar and communications designs. The AWG4000 Series is the first waveform generator with the flexibility to meet such a broad set of requirements. As a signal generator AWG4000 offers two analogue channels, up to 2.5 Gsamples/sec sampling rate, 750 MHz bandwidth, 14-bit vertical resolution, up to 64 Mpt/ch arbitrary memory, sequence with up to 16,384 entries, and 32-bit digital channels. Many of the specifications can be upgraded in the field, including memory and digital outputs. The AWG weighs less than 15 pounds and incorporates a 10.1-in. touch screen. For simple tasks, the AWG4000 offers a basic arbitrary/function generation (AFG) user interface for generating function and arb waveforms with a minimum number of button clicks and a shallow menu hierarchy on the 10.1-in. Touch screen. For more complicated tasks, the instrument offers an advanced Windows-based user interface that can be used to generate complex sequences and modulated signals in parallel with digital outputs. Signal generation tools such as RFXpress or Matlab can also be installed locally.

Tektronix
www.tek.com/awg4000

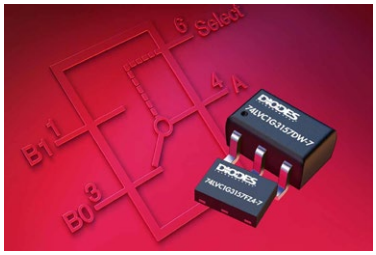
Smart force sensor design operates as both weigh scale, touch interface

Design engineers can now rapidly evaluate and deploy new human-machine interface (HMI) devices using the MAXREFDES82# smart force sensor reference design from Maxim Integrated (San Jose, CA). While typical weigh scales provide one dimension of information, the downward force, the MAXREFDES82# reference design provides both downward force and centre of mass. It does so by collecting responses from four load cells using the MAX11254, a 24-bit, 6-channel analog-to-digital converter (ADC). This unique configuration, enabled by the highly integrated 24-bit ADC, provides second and third dimensions of information about whatever object presses upon it. The chip's 64-ksps capability provides real-time operation with accurate measurements of weight and centre of mass up to 780g. The interface requires no special glass or material, making it suitable for industrial environments

Maxim Integrated
www.maximintegrated.com

Audio multiplexing SPDT switch has low losses

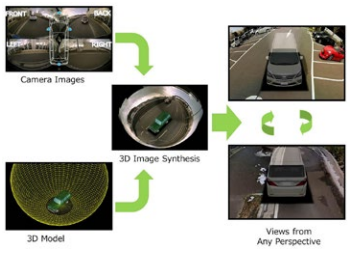
The 74LVC1G3157 single-pole, double-throw analogue switch (Diodes Inc.) is designed for multiplexing digital or analogue signals. Its low on-state resistance ensures high integrity when routing audio signals, for consumer electronics from cell phones, tablets and e-readers to personal music players, hand-held games, satellite navigation and other audio equipment. With an on-state resistance of less than 6Ω when operated with a 5V supply, the IC enables the routing of input audio signals and can support output routing in low-power applications. Its typical off-state leakage current of 20 nA provides a high degree of isolation, allowing components such as resistors and capacitors to be switched in or out of the signal path for programmable filters or different gain configurations. The 74LVC1G3157 is designed for a 1.65V to 5.5V power supply range and can handle signal amplitudes between VCC and ground. The control input can be up to 5.5V regardless of VCC and the control pin includes hysteresis to allow for slower input rise and fall times. The X2-DFN1410 package occupies 1.4 mm ^{2} of board space, allowing designers to use multiple parts to route multiple signals while the 0.5 mm lead pitch eases board assembly. This device is also available in SOT363 package.



Diodes
www.diodes.com

360° wrap-around view evaluation package for all

Socionext has introduced a new evaluation solution package for its 360° Wrap-Around View (WAV) system. The package combines the hardware, software and support services necessary for initial evaluation and development of the WAV system. The company aims to expand the use of its 360° WAV system into both the automotive and the non-automotive applications, with cameras facing forward, backward, left and right to synthesize images on a three-dimensional model, then generating the views around the vehicle. While conventional systems only synthesize images on a two-dimensional model and can only provide a view from a certain fixed viewpoint, such as from the top, the WAV thre3D model can display views around the vehicle from any perspective, making it useful for parking assistance and other applications such as lane change while driving. The system can enhance situational awareness for operators of construction vehicles.

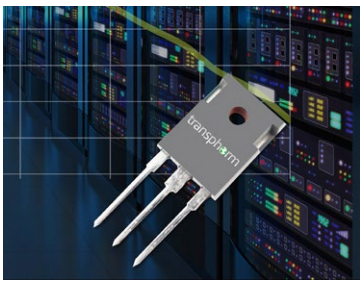


Socionext expects this new solution will help accelerate the spread of 360° WAV system into broader visual-aid applications, including non-automotive fields such as aerial shooting using drones.

Socionext
www.socionext.com

650V GaN FET, low on-resistance, in TO-247 package

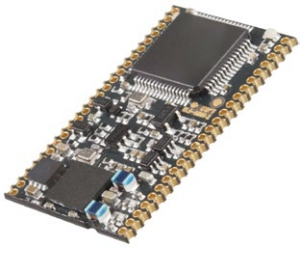
Gallium nitride device maker Transphorm recently introduced what it positions as the industry's only fully-qualified 650V-rated FET, in 'conventional' packaging. It claims the lowest R(on) of any such device at 41mOhm; and ultra-low Qrr of 175 nC to increase power density and achieve higher efficiencies over a broad range of power levels. Why TO-247? Transphorm acknowledges that to fully exploit the potential of GaN, there is an argument for more advanced packing [with lower inherent inductance]. However, the company says that to get designers working with GaN, the company has opted for a package that designer know and trust. There is a great deal of benefit to be gained from switching to GaN and moving from switching frequencies of, say, 10-20 kHz to 50 to 70 kHz, "It doesn't need to be 300 kHz [to see worthwhile gains]". Transphorm sees a great deal of design activity around the adaptor market; external PSUs that operate in a tightly-regulated environment and where size and efficiency gains are always welcome. The TPH3207WS GaN FET claims lowest on-resistance (41 mOhm) in a TO-247 package that reduces system volume as much as 50% without sacrificing efficiency. The device's low Rds(on) and ultra-low Qrr (175 nC) bring the benefits of GaN to applications that previously relied on silicon, enabling engineers to achieve power-dense solutions with reduced component count and improved reliability in high-voltage power conversion applications. The TPH3207 improves system reliability, performance and power density in an easy-to-handle cascode configuration.



Transphorm
www.transphormusa.com

Multi-standard reader RFID reader is only 31x17.8x2.5mm

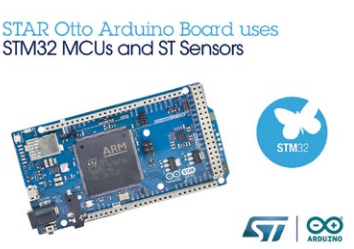
Elatec RFID Systems's TWN4 MultiTech Nano is an RFID/NFC reader unit supporting all of the common RFID technologies for 125 kHz, 134.2 kHz and 13.56 MHz frequencies, packed in a 31x17.8x2.5mm footprint. With the components mounted to one side, it facilitates easy placement on the main circuit board. A version with pins already soldered is also offered for quicker implementation. Thanks to its minimal size, variety of external antennae options and expanded temperature range, TWN4 MultiTech Nano is particularly well suited for industrial and mobile applications. Elatec can provide reference plans for the antenna design and design kits upon request. This RFID reader is NFC capable, making it a strong choice for applications that involve communication with smartphones. An EMVCo certification for payment applications can be obtained optionally.



Elatec GmbH
www.elatec-rfid.com

Arduino baseboard targets high performance graphics for IoT

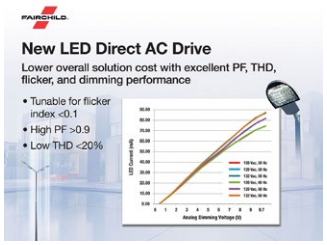
A collaboration between the Arduino open-source platform maker and STMicroelectronics yields the first Arduino board based on the STM32 ARM Cortex-M MCU, which offers high-performance graphics, TFT touch display, wireless link, and connectivity for audio, MicroSD, USB OTG, and camera. The agreement makes the STM32 family of microcontrollers, along with ST's full portfolio of sensing, power, and connectivity technology, more accessible to the Arduino maker community. The first product of the STAR (ST and Arduino) program is the STM32F469-based STAR Otto baseboard, allowing IoT developers to build high-performance graphics into their smart devices using accessible hardware and software to improve their applications with easy-to-use touch displays and audio for command and control as well as for media-streaming use cases. STAR Otto is built around the 32-bit STM32F469 MCU, which includes ST's Chrom-ART graphics accelerator and MIPI DSI display interface along with an open-source software graphics library. STAR Otto provides a pre-integrated wireless link and audio capabilities, enabled by an ST MEMS microphone together with the necessary open-source drivers.



Arduino
www.arduino.org

Simpler LED lighting with direct-AC-drive chips

Fairchild's FL77944 is the first product in an LED Direct AC Drive family of solid-state LED lighting solutions that manufacturers can use to scale power and create smart and scalable LED-based lighting products that can be smaller, have higher performance and a longer system lifetime compared to products using the switch mode power supply (SMPS) approach. LED direct AC drive has only had limited use, Fairchild says, because of the issue flicker (at mains frequency). This product, the company says, can reduce the flicker effect and allow the concept to be applied to commercial and industrial lighting. The IC offers good power factor and total harmonic distortion of under 20%; it supports dimming by analogue and pulse width modulation and can scale from 10 to 120W lighting systems, by parallel connection. Flicker is specified by the peak-to-average ratio of the light emitted. The IC can be operated without energy storage (that smooths the dips in the light level) in which case it delivers a flicker factor of around 0.3; by adding four, 100 µF capacitors, this can be reduced to under 0.15, as demanded by commercial applications. The FL77944 has all the important dimming capabilities required for smart lighting products, including phase-cut dimming as well as analog and PWM dimming, which is also key for wirelessly connected lighting.



Fairchild
www.fairchildsemi.com

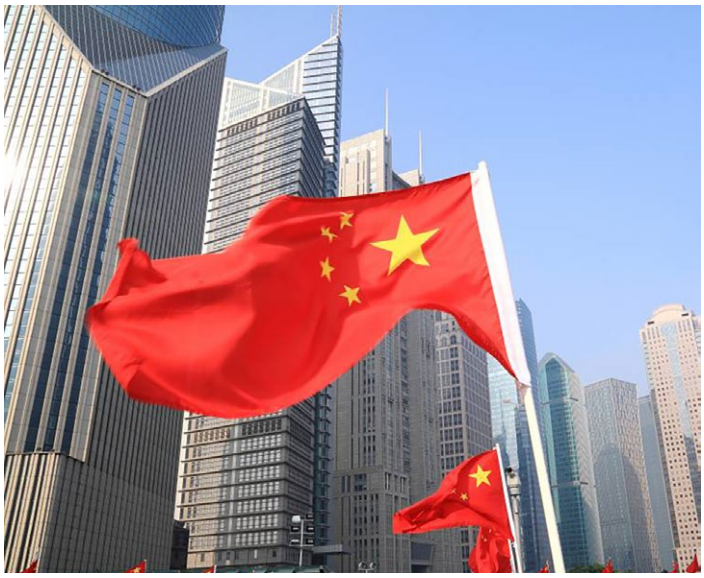
The only two things that matter for digital companies in China

By Michael Wade

I recently spent a week visiting companies in China, trying to learn as much as I could about digital transformation and trends in that country. I suspected that there were major differences between how digitization was viewed in China versus the West.

There were.

As I visited large corporations like Didi Chuxing (the Chinese competitor to Uber that last week received an injection of $1 Billion in funding from Apple), as well as mid-size companies and startups, I learned that only two things matter to Chinese digital executives: scale and speed. All else is secondary. Simply put, they want to get really big, really fast.



Culturally, we might liken it to the Chinese game of Go. Go, unlike relatively complex Western games like Chess, is a straightforward battle for territory. The player who controls the majority of the board at the end, wins. The Chinese digital landscape today is comparable to a game of Go.

Scale and speed make life interesting in China. Yet, in the race for space, many traditional aspects of business are being sacrificed, like revenues, profits, and operational rigour. Cheap money, massive organic growth, and friendly government policies are hiding a multitude of operational sins.

Unfortunately, Chinese firms are not alone in this. Plenty of Western unicorns (privately held firms valued at $1billion or more) are following a similar strategy: get scale first, worry about revenues and profits later. Facebook and Google have spectacularly shown how this business approach can work. But, these are the exceptions. Companies such as Snapchat, Twitter, and LinkedIn have gained scale, but are still struggling to build solid business cases. Many others have failed, or will fail.

Indeed, failure is on the minds of Western digital firms. Many remember the dot.com bubble of the late nineties and its subsequent collapse. Even if their memories do not stretch that far, the financial crisis of 2007-2009 is hard to overlook. Western tech investors are (thankfully) starting to look much more closely at business model sustainability today.

By contrast, Chinese companies have only known growth and success. There was no dot.com collapse in China, and the financial crisis was barely a blip on the Western horizon. Chinese growth continued unabated. Chinese businesses do not fear failure, because they have never felt its sting. This is great for innovation, and make no mistake, there is massive innovation happening in China today, but it can lead to economic recklessness.

Michael Wade is the Cisco Chair in Digital Business Transformation, and Professor of Innovation and Strategic Information Management at IMD - www.imd.org

The role models do not help. In China, successful digital giants cast a long shadow. Alibaba and its founder Jack Ma, for instance, are revered in China, which was clearly evident when I visited the company's headquarters in Hangzhou – a city half a step behind Shanghai, Beijing and Shenzhen in the Chinese urban hierarchy.

Alibaba is impressive to be sure. It embodies both the speed and scale that Chinese businesses aspire to reach. The company grew by providing great services at no cost. It vanquished eBay in China by not charging the buyer or the seller to conduct business on its Taobao marketplace. Free services are hard to compete against. Even today, Alibaba makes relatively little revenue ($3.7B in the most recent quarter vs $29B for Amazon and $18B for Google), considering the gross merchandise volumes of goods and services sold across its various marketplaces ($113B in the most recent quarter).

The Chinese businesses and entrepreneurs I met consistently cited Alibaba as a model for success. Alibaba is big, fast, and profitable. The problem is that it is only profitable because it is big. Alibaba, Tencent, and Baidu (the Chinese BAT digital giants) are winning the game of Go in China. Scale benefits matter, but not everyone can be so big. The BATs are succeeding because they can take razor thin margins on very large numbers of transactions, or because they can subsidize free services in one area with paid services in another. However, as Chinese consumers get more and more accustomed to very low prices, free services, and huge discounts, it makes it more difficult for others to compete.

This situation cannot last forever, or can it?

I have called for a correction in Western digital markets, and one might expect the same to happen in China. However, there is one important difference in China that argues against it. The government is unabashedly pumping money into the commercial sector.

During my recent visit, I heard multiple stories of local, regional, and national government agencies subsidizing labour, rent, and providing cheap business loans. Very few of the companies I visited were making a profit. Some seemed confused by the question! As long as the government props these companies up, they will continue to exist.

A cavalier attitude to commerce, combined with attractive incentives, and a so-so grasp of business fundamentals is a dangerous mix. The Chinese digitization growth story is impressive, to be sure, but it is not sustainable without generous and persistent government intervention.

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DISTRIBUTION CORNER

pi-top kit in stock at RS Components

RS Components is extending its portfolio of processor board development kits with the addition of the competitively priced pi-top 'build your own laptop' kit. Launched in a Kick-starter campaign, the pi-top concept is essentially a Raspberry Pi powered laptop enabling students to learn about programming, computing and hardware creation including electronics fabrication. It also teaches students transferable skills that will help them to create their own hacker and maker hardware projects. With no need for a soldering iron, the pi-top concept allows users to quickly start to experiment with electronics, create PCBs and produce 3D printing projects such as a pi-top case. This is facilitated through step-by-step online tutorials and lesson plans in a cloud-based learning model.

RS Components
www.rs-online.com

Sensor-to-cloud platform accelerates IoT applications

Farnell element14 and Sierra Wireless have jointly launched the mangOH Green Open Hardware IoT Platform and the mangOH kit, allowing developers to test and prototype their IoT ideas to market within weeks. The sensor-to-cloud platform provides an all-in-one hardware, software and cloud-based solution for industrial IoT applications. At the heart of the board are two industrial-grade CF3 connectors to enable the use of either an AirPrime HL Series module or an AirPrime WP Series applications processor module from Sierra Wireless. The AirPrime WP Series cellular modem provides the device-to-cloud architecture enabling IoT developers to build a Linux-based product on a single module.

Farnell element14
www.element14.com/designcenter

zero lead-time, zero start-up cost promises Anglia

Distributor Anglia Components has launched Anglia 80/20, an intelligent inventory management service offering electronics manufacturers a flexible, instantly accessible inventory of commodity components on an invoice at usage basis to support their growth. The new service aims to give SMEs the competitive advantage they need to compete with high volume manufacturers. Anglia 80/20 is said to offer a new level of flexibility in the supply chain through consignment/Vendor Managed Inventory (VMI). There is no start-up cost as participating customers receive an agreed level of inventory on their regularly used commodity components that are held on their site. Customers are issued with a free starter pack including a wireless 2D scanner and barcoded user cards for security, which allow selective authority levels and auditable user information.

Anglia Components
http://8020.anglia.com

Lumileds signs Arrow Electronics for global distribution

Lumileds and Arrow Electronics announced a strategic agreement for the global distribution of Lumileds comprehensive portfolio of application optimized LEDs including high power, mid power, low power, CoB, color and UV LEDs as well as the infinitely configurable Matrix Platform. The agreement aligns with both companies' dedication to providing customers with responsive, accelerated service and reliable, high performance solutions. "Lighting is an extremely dynamic market and today's lighting producers expect timely delivery of the right LEDs where and when they are needed," said Emmanuel Dieppedalle, Senior Vice President of Marketing and Sales at Lumileds.

Arrow Electronics
www.arrow.com

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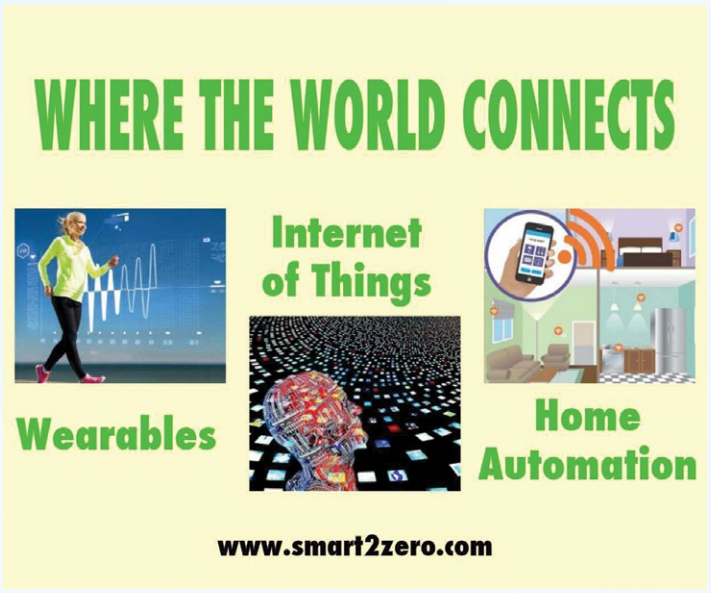

www.smart2zero.com

www.electronics-eetimes.com/newsletters

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www.microwave-eetimes.com/

www.eetsearch.com

CoolMOS™ CE in SOT-223 package

Cost-effective drop-in replacement for DPAK

Infineon is growing the portfolio of CoolMOS™ CE with the SOT-223 package as a cost effective alternative to DPAK that also enables footprint reduction in some designs. The package can be placed on a typical DPAK footprint and comes with only a small compromise in thermal behavior. The SOT-223 from Infineon targets LED lighting and mobile charger applications.

The SOT-223 package without middle pin is fully compatible to the footprint of a DPAK and therefore allows one-on-one drop-in replacements and second sourcing.

Key features and benefits

- Drop-in replacement for DPAK at lower cost
- Space savings in designs with low power dissipation
- Comparable thermal behavior to DPAK

To learn more, please visit:
www.infineon.com/sot-223